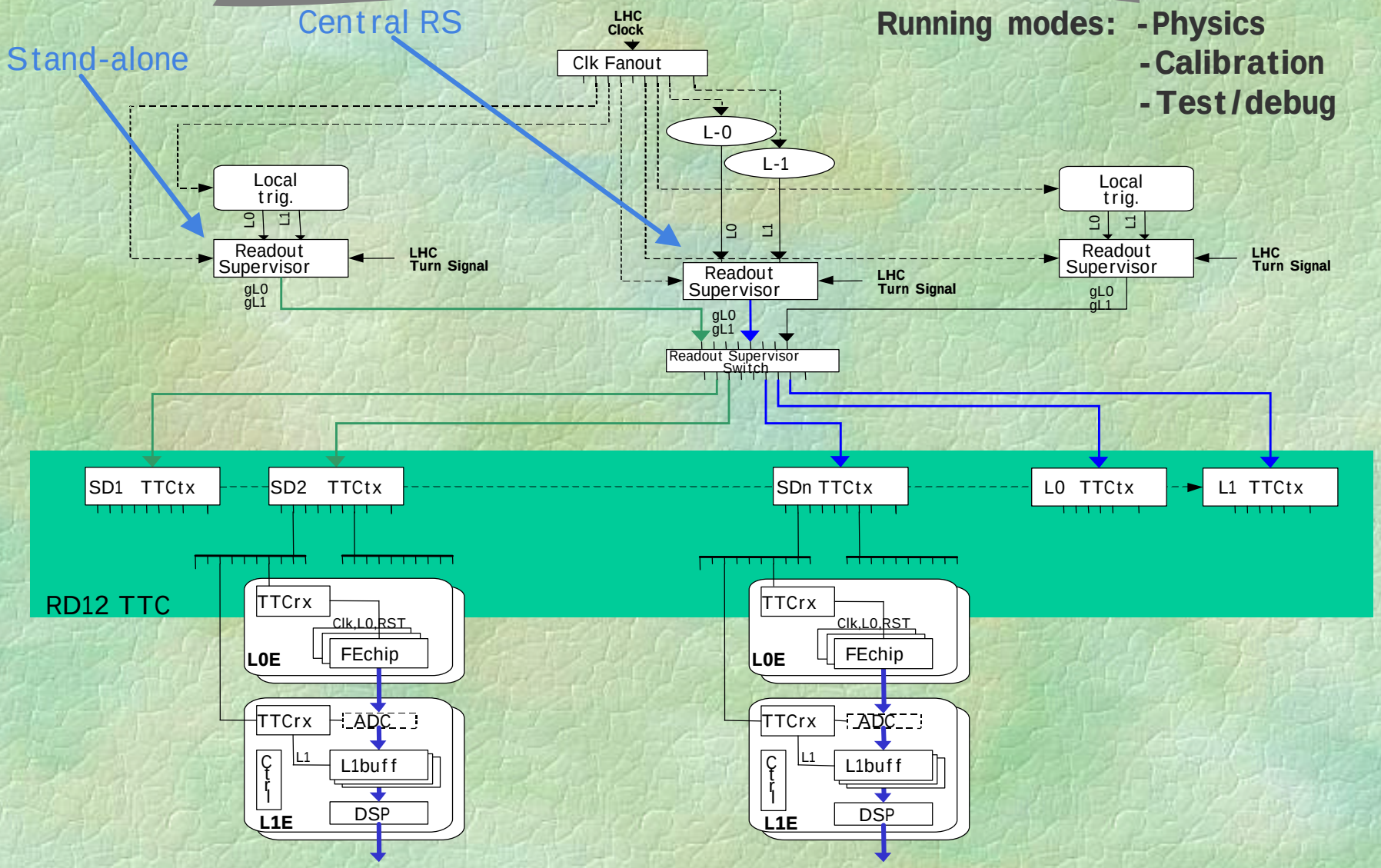
- Readout Supervisor -

Outline

- Readout Supervisor rôle and design philosophy
- Trigger distribution
- Throttling and buffer control
- BCRs & Resets
- Auto-triggering for calibration & test
- Priority scheme between L1/resets/commands
- Errors detected by RS
- Counters
- RS data block
- Discussion topics

Note: No recipes just flexible machinery! Feedback!

Readout Architecture



Running modes:
- **Physics**
- **Calibration**
- **Test/debug**

Design philosophy

- Flexible and versatile
- Simple
- No internal intelligence --> configured by ECS
- Accounting
- Transparent --> debugging
- Reliable

Specifications

RS Design Specification document underway:

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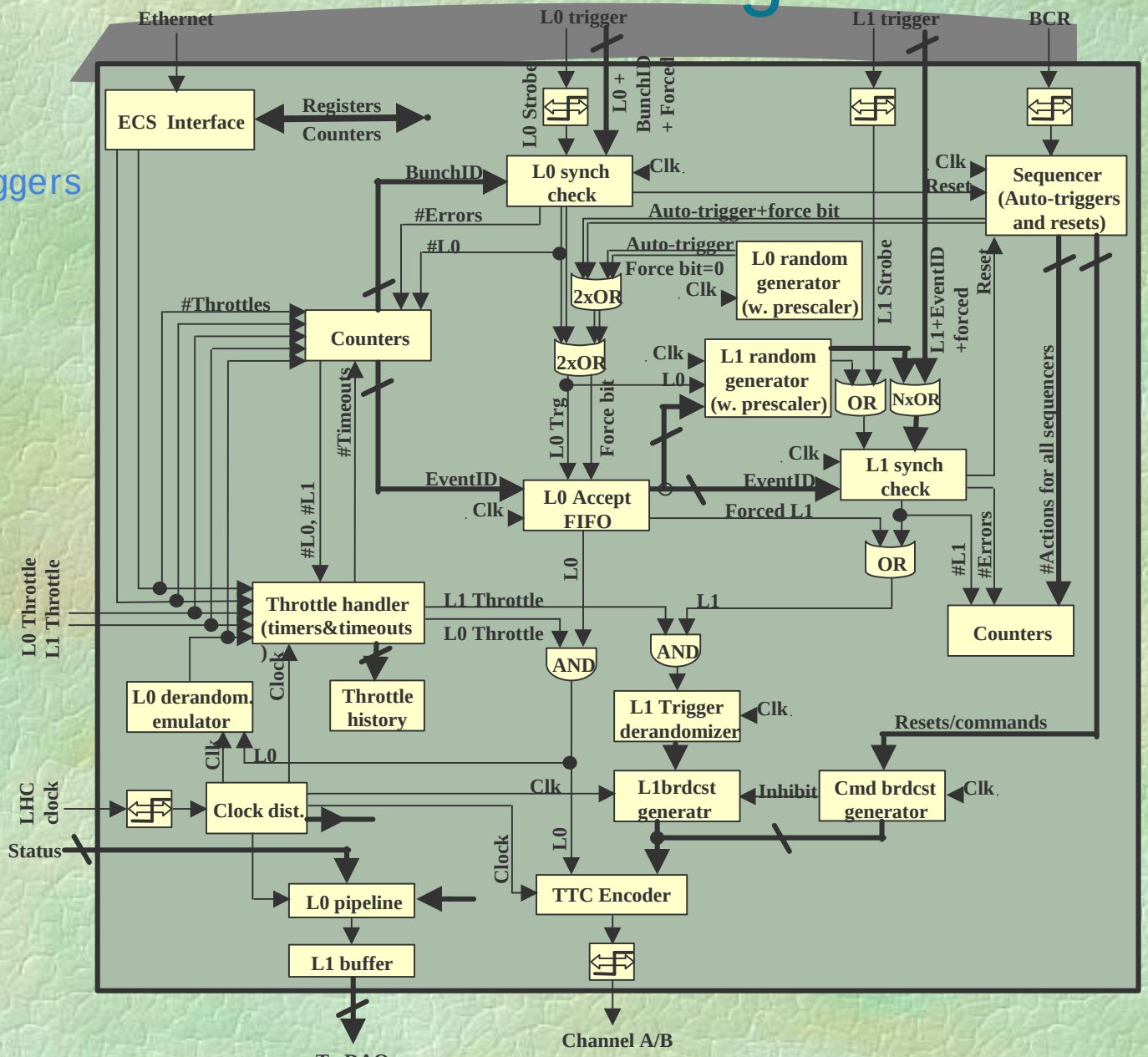
RS block diagram

- Forcing triggers



Throttling and buffer control

Overflows:

- L0 de-randomizer emulated --> internal L0 throttle
- L1 trigger system --> hardwired L0 throttle
- L1 derandomizer --> throttle central or cabled
  - central assumes fixed length zero-suppression
  - cabled to RS means FE monitoring + cabling
- Front-End Multiplexing or Readout Units --> hardwired L1 throttle
- Subfarm Controllers --> L1 software L1 throttle via ECS

Counters, timers, time-outs and history buffer for throttles

- On time-outs --> ECS interface raise alarm with throttle type

Count dead-time and losses

BCRs and Resets

- Sequencers to implement the various resets:
  - Bunch Counter reset

  Programmable timing:
  - Reset L0 pipeline+derandomizer at regular intervals in phase with orbit signal
  - Reset L1 FE at regular intervals in phase with orbit signal
  - Single resets triggered by ECS, transmitted at pre-specified cycle

- BCR highest priority
  - BCR + other resets simultaneously

Calibration & test

- Programmable sequencers
- Forcing auto-triggers
- Available online and stand-alone
- Auto-triggering:
  - Pre-defined intervals -- pedestals etc
  - Consecutive bunch sampling -- timing
  - On calibration pulse -- fired by TTC command
  - Random trigger -- minimum bias
- Stand-alone calibration
  - All of the above
- Stand-alone test with or without local trigger
  - Pre-scalable L0 random trigger (max 1.5 MHz, Poisson)
  - Pre-scalable L1 random trigger (max 200 kHz, Poisson)

Channel B priority scheme

- Priority scheme on channel B:
  - 1) Resets / Auto-triggers / commands
  - 2) L1 decisions
- Reset / auto-triggers / commands --> equal priority
  - Sequencer time structure checked before down-load to prevent conflicts (software)

Errors detected by RS

- Errors:
  - L0 strobe missing
  - L0 de-synchronization
  - L1 missing (max latency exceeded?)
  - L1 de-synchronization
  - Buffer overflows
  - Throttle time-outs

} ECS interface raise alarm
Optional: reject + direct reset

- Initially mark&keep erroneous events, later configure automatic rejection/recovery

Counters

- LHC bunch clock
- LHC orbit clock
- Bunch ID
- Event ID
- L0 accepts
- L1 accepts
- Missing L0 strobes
- L0 bunch ID error
- L1 event ID error
- L0 derandom. overflows (internal L0 throttle)
- L0 HW throttles
- L1 HW throttles
- L0 SW throttles
- L1 SW throttles
- Bunch crossings lost during L0 throttle
- L0 yes's converted to no's during each type of throttle
- L1 yes's converted to no's during each type of throttle
- Throttle time-outs

- Resets (different levels)
- Bunch crossings lost during resets
- L0 yes's converted to no's during resets
- L1 yes's converted to no's during resets
- Forced level-0 accepts
- Forced level-1 accepts
- Self-triggers generated by sequencers

•ECS interface polls over counters and status registers to monitor and alarm

RS data block

- Readout Supervisor “Front-End” handles the RS data block:
  - Bunch ID
  - Event ID
  - Status information provided through front-panel input
  - Event type (physics, random, calibration, empty crossing, test, special)
  - Level-0 and level-1 force bits
  - Error blocklet

Interfaces

Input/output	In/Out	Specification	Type
BC in	In	LHC bunch clock from TTCmi	Lemo
BC out	Out	LHC bunch clock output	Lemo
BCR in	In	LHC turn signal from TTCmi	Lemo
BCR out	Out	LHC turn signal output	Lemo
L0 in	In	L0 trigger decision with 12-bit bunch id + forced L0 bit + strobe	17-pin parallel
L0 in (aux)	In	Auxiliary L0 trigger from any source	Lemo
L0 out	Out	L0 trigger decision output for monitoring	Lemo
L1 in	In	L1 trigger decision with 12-bit event id + forced L1 bit + strobe	17-pin parallel
L1 out	Out	L1 trigger decision output for monitoring	Lemo
TTC out	Out	Channel A/B encoded and serialized	1 or 2 Lemo ?
Throttle L0 in	In	L0 throttle input, eg from L1 trigger system	
Throttle L0 out	Out	L0 throttle output for monitoring	
Throttle L1 in	In	L1 throttle input, eg from L1E	
Throttle L1 out	Out	L1 throttle output for monitoring	
Status in	In	Status information + strobe	130-pin parallel?
RS data	Out	RS data to DAQ	S-link
Ethernet	In/out	ECS interface	Ethernet

LED	Specification	Colour
On/Off	Power on	Green
BC ext	External bunch clock present	
BC int	Internal bunch clock used	
BCR ext	External orbit clock present	
BCR int	Internal orbit clock used	
L0	L0 trigger present	
L1	L1 trigger present	
Thrtl L0	L0 throttle asserted, stretched on-time	
Thrtl L1	L1 throttle asserted, stretched on-time	

Conclusions

- Specifications well underway
- Need feedback about additional features and requirements

- First functional and modular specifications to be finalized
  - ~2 months
- Simulation
- Design and prototype 12 - 15 months

Discussion topics

- Command broadcast (non-addressed)
- Addressed commands (individual TTCrx)
- L1 derandomizer throttle, central or cabled
  - central assumes fixed length zero-suppression
  - cabled to RS means FE monitor + cabling
- Freezing bunch clock -- debugging
- How many Readout Supervisors?
- Jitter requirements for Readout Supervisor (TTCex)
- L0 rejects before reset to empty L0 derandomizer?
- L0 latency within RS