LHCb xxxx-xx

DAQ

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The SPECS SLAVE mezzanine board

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ABSTRACT

This document attempts to describe the SPECS SLAVE mezzanine board designed for LHCb. The technical specifications of the bus itself are given in another document [1]. This note presents how the mezzanine board has to be interfaced within the various sub-systems of LHCb.

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1. Context

The SPECS has been designed to permit control of the front-end electronics of LHCb. The system mostly consists of three elements : a bus master located on a PCI board in the counting room (see fig 1), a slave in the cavern, delivering JTAG, I2C and a parallel interface to control the electronics, plus dedicated software to drive the system from the PVSS II SCADA environment upon which the LHCb ECS system is built.

The prototype board housing the masters is shown on fig 1. It's a PCI board providing 4 RJ45 outputs. Two of them are mixed, which allows the users to drive JTAG or I2C directly from their PC for test bench purpose (for instance). As a slave is integrated within the board, the system behaves like the expanded one. In particular, the software is identical. On the first prototype of the board (Firmware version 1.0), the mixed outputs don't provide SPECS but only I2C or JTAG.

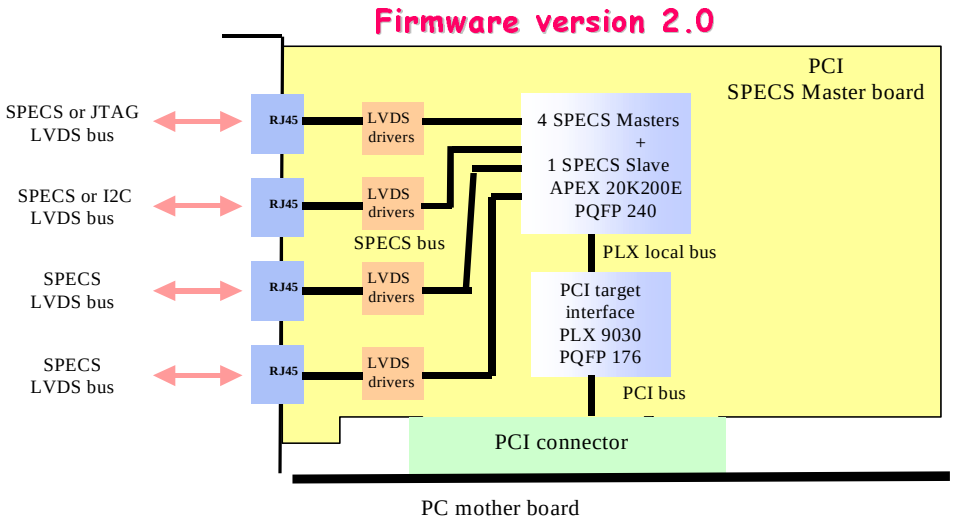


Fig 1 : the SPECS prototype PCI master board.

The protocol between master and slave(s) is described in ref[1] and are not too relevant here. The main discussion here concerns indeed the location of the slave, and the types of bus it can deliver.

The slave will be designed as a portable Verilog code and eventually physically integrated in an ACTEL anti-fuse PGA. With this technology, the slave will be SEL immune, and will also be made SEU immune, provided the internal registers will appropriately be protected by triple voting techniques, whereas states machines will use one-hot state. Moreover, to ensure a high reliability to the decoding of the SPECS commands, there will be no state machine in the SPECS receiver part. In addition thereto, all commands (and in particular all the resets) will be generated without using any local clock, only the SPECS lines. This may for instance allow the user to reset the TTCrx through SPECS if necessary. The chip will also be reasonably radiation tolerant, up to 10 krads (with some safety factor, the ACTEL chip having been tested up to 40 krads) over the lifetime of the experiment. It can then be placed at most locations where we foresee to have electronics, except in or near the Velo tank. Fig 2 shows the block diagram of the slave's interconnections. It may also be envisaged by users to use the slave Verilog code as a block within a bigger Actel FPGA, even if this makes the SPECS interfacing much trickier.

Figure 2 shows a block diagram of the SPECS slave chip. As it appears on the left, the SPECS bus is bi-directional, two electrical pairs being dedicated to each direction. On the top side, one can find the different control signals necessary for a proper functioning. On the right side, the parallel I/Os are represented together with the service functions. Finally, the bottom side describes the JTAG and I2C dedicated I/Os.

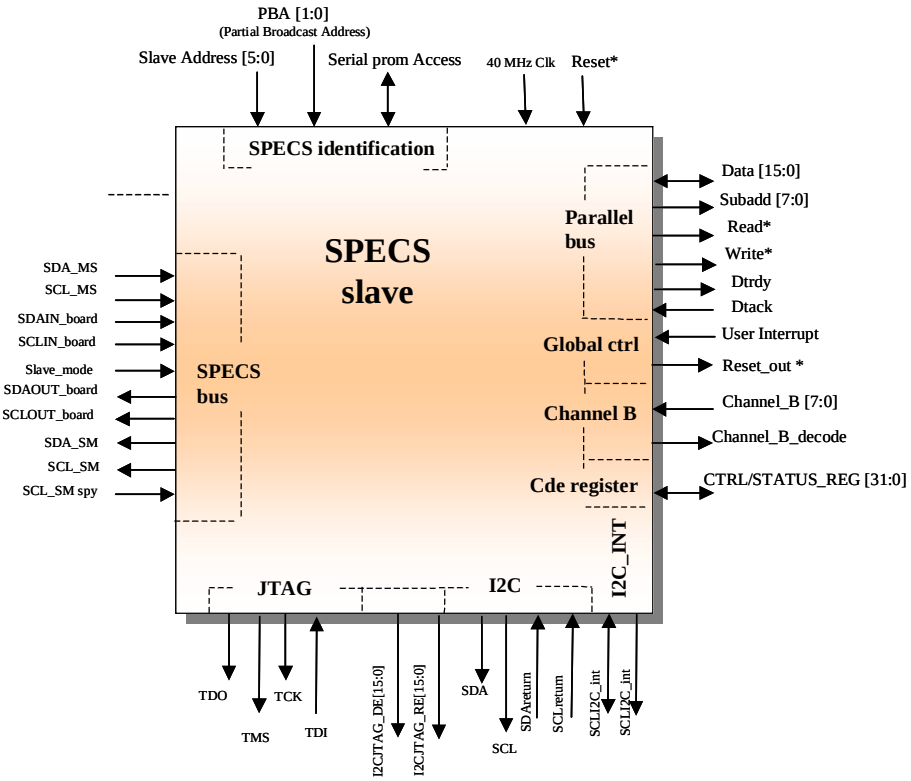


Fig 2 : the SPECS slave chip.

Because of the potential radiation environment, we will use for the series version anti-fuse FPGAs of AX ACTEL family. These components have been tested in radiation (LHCb note [3]) . For the mezzanine prototype board, we'll use a SRAM based FPGA (ALTERA APEX).

2. SPECS slave mezzanine general description.

In this solution, an intermediate mezzanine board (see fig 3) provided by LAL-Orsay, houses the SPECS slave, and provides JTAG and I2C. One can implement on its board up to 16 JTAG or I2C outputs if necessary (therefore, use the proper cabling as described on fig 10 & 11). The SPECS system is seen in this case as a JTAG or I2C provider, and its internal features can be completely ignored. The use of the long distance differential I2C and JTAG provided by the SPECS slave is mandatory for boards situated in high radiation areas, like the Velo detector boards, for it isn't possible to put the SPECS FPGA at these locations. The mezzanine board will also provide most of the necessary service functions for the sub-detector front-end electronics. The goal is to avoid to put unnecessary electronics in the radiation sensitive area.

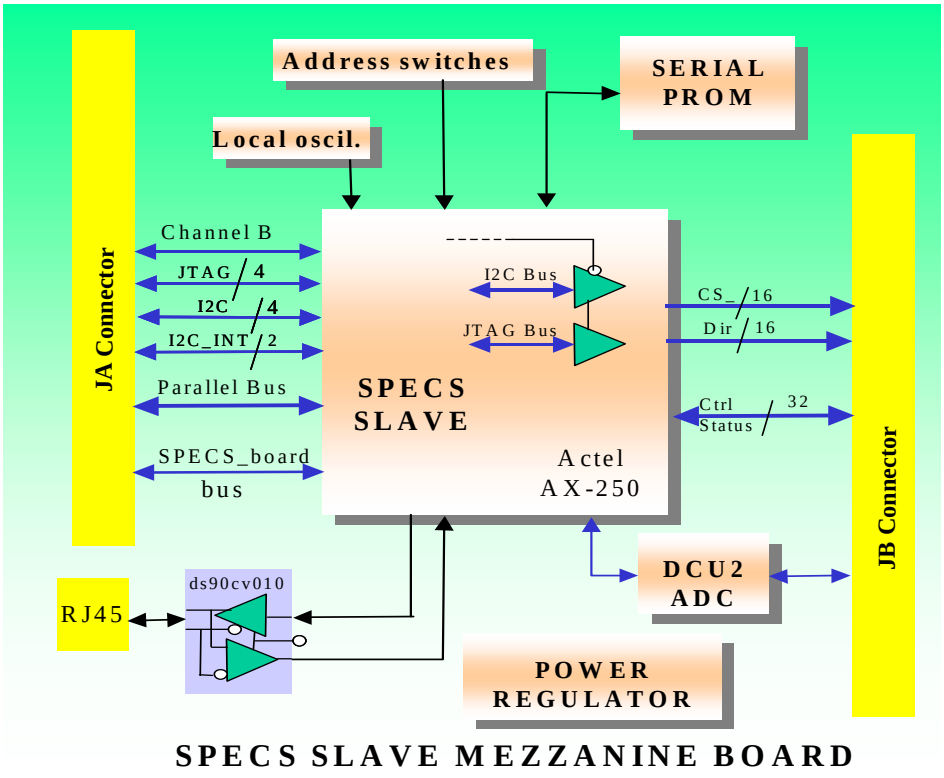


Fig 3 : SPECS slave mezzanine board.

List of the features of the mezzanine board:

- One long distance point to point differential SPECS interface (from SPECS master).
- One unipolar SPECS local interface for multi-load bus application.
- One output for long distance I2C.
- 16 I2C/JTAG chip-select control bits for external drivers.
- 16 I2C/JTAG direction control bits for external drivers.
- One local I2C bus.

- One JTAG bus.

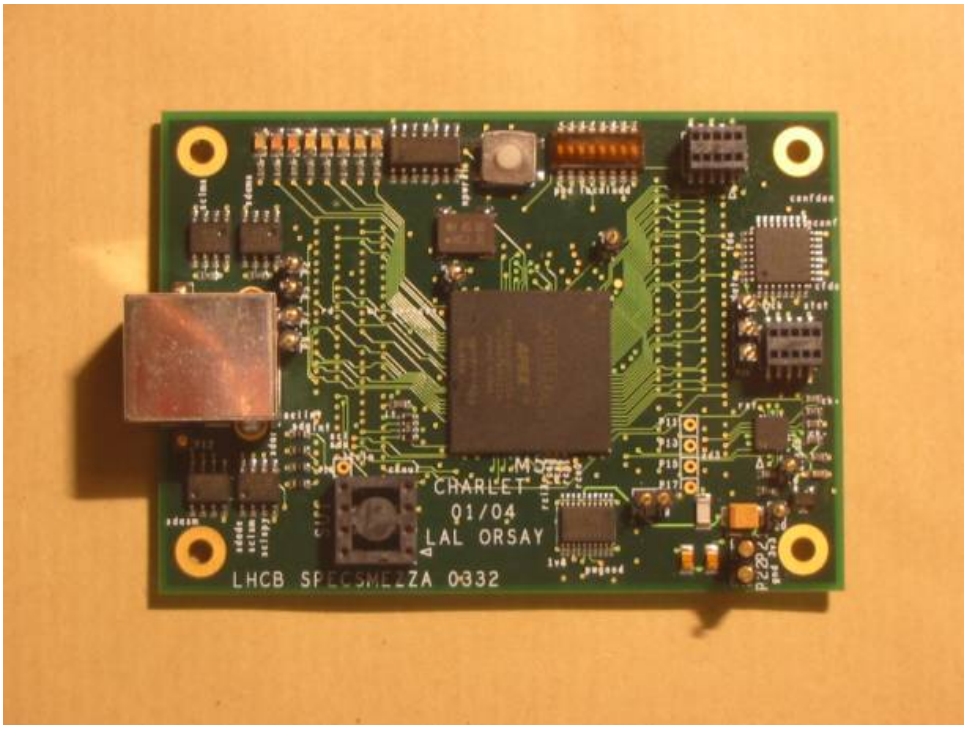


Fig 4 : the SPECS slave mezzanine prototype board.

- One parallel bus offering 16 data bits & 8 Address bits.
- One decoder for the channel B of the TTCrx will be implemented within the SPECS slave chip. It will decode the necessary functions (currently L0 counter reset and Test pulse).
- One 32-bit static register to control or read back the local environment. The bits [32:24] can be individually configured either as an output or as an input. As an input, they may be configured as an interrupt vector, each of them being then able to generate an SPECS interrupt. The bits [23:0] can individually be programmed as input or output. This register does not need any external clock to get written by SPECS. After a hardware reset, each of these I/Os becomes an input by default for safety reasons.
- One reset signal. This output can be triggered without the need of any clock on the board.
- One local 40MHz oscillator. It is also provided as an output of the mezzanine and can be enabled by software. In case of LHC clock failure, it automatically replaces the LHC clock to allow the read-back over the SPECS bus.
- One PROM which will allow the ECS system to get information about the front-end element housing the mezzanine. It will be mounted on a socket.
- One DCU2 chip with 6 ADC channels of 12 bits resolution
- 6 switches will be available to fix the SPECS slave address and 2 to fix the broadcast group address (one per type of board for instance).

3. Mezzanine physical implementation

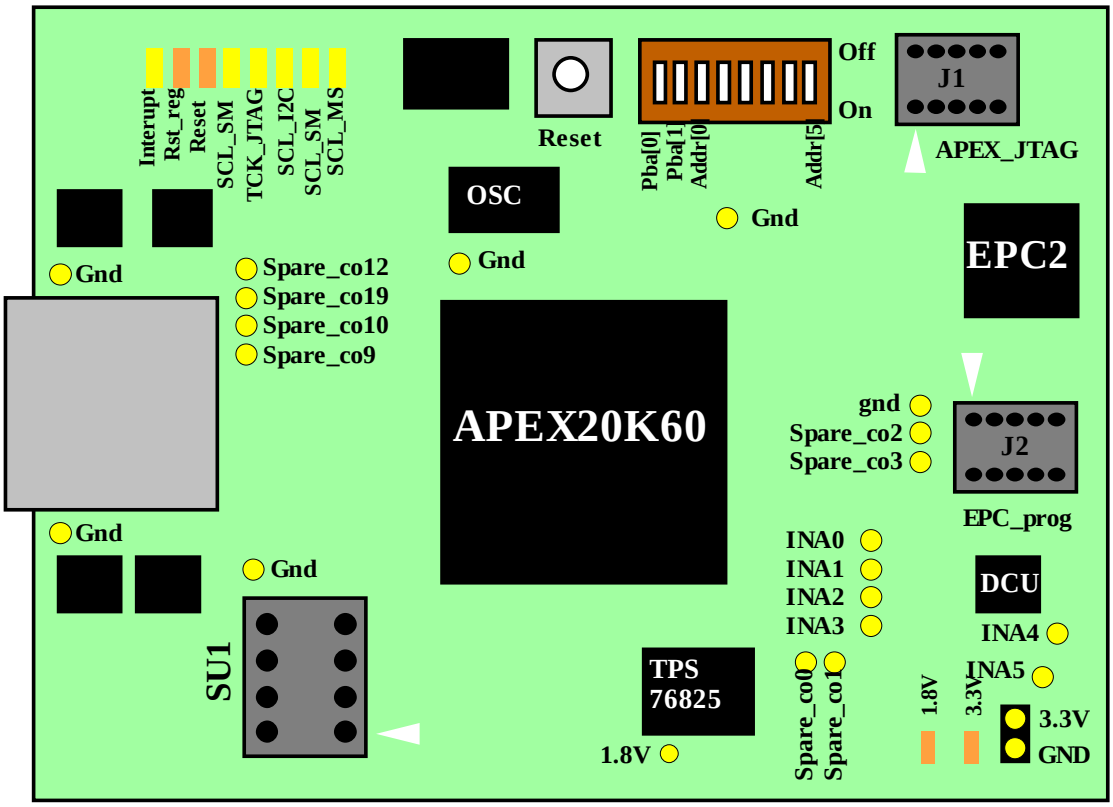


Fig 5 : SPECS Mezzanine physical implementation

4. SPECS remote bus implementation

a. SPECS bus

As described in the note [1], the SPECS protocol's type is mono-master multi-slave. This permits implementation of many slave on the same bus. This is the solution we intend to use in the calorimeter. The SPECS bus will actually be distributed on the remote crate backplane by the so-called Crate Controller board (CROC), which also takes care of the TTC signals for all the boards in the crate (see Fig 5). This allows us to ensure a perfect integrity to the signals. This dedicated backplane already exists, and is potentially available for use by other detectors. (See ref[2])

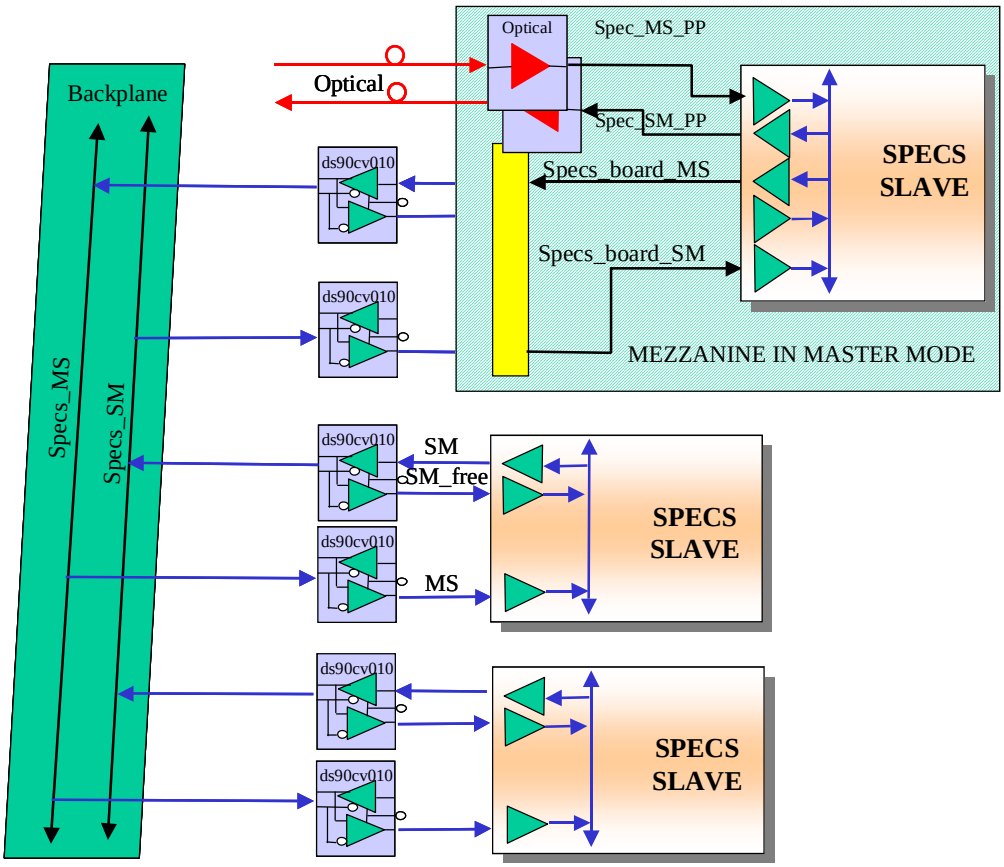


Fig 6 : SPECS bus implementation for the calorimeter.

In this implementation, a mezzanine mounted on the CROC board (configured in master mode) forwards the SPECS bus towards all the other boards in the crate. These house their own SPECS interface, in this case integrated in an ACTEL FPGA which is shared with other logics.

b. I2C bus

Fig 6 displays the physical implementation of a remote I2C bus. In this case, one needs to implement drivers on the board to bufferize the signals and to select which I2C bus is on duty. For long distance and irradiated environment, we recommend DS92LV010A or SN65LVDM176, both having been tested in radiation (LHCb note [4]).

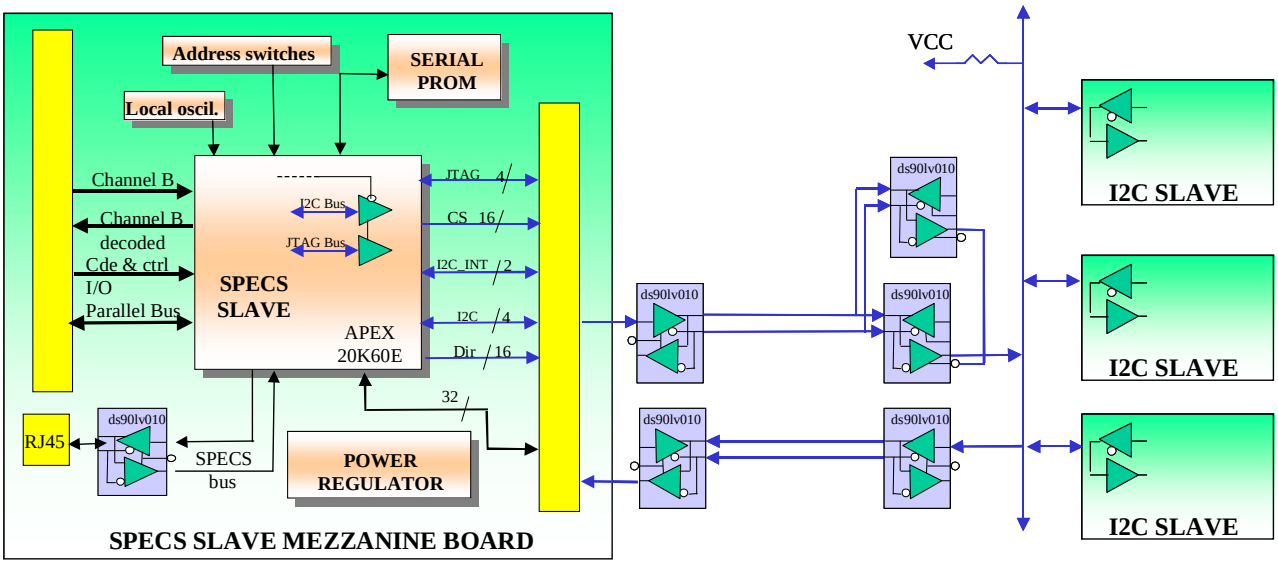


Fig 7 : physical implementation long distance I2C bus.

For those long distance busses, we also recommend to use cat5 cable with RJ45 plugs. To permit using standard Ethernet cable and to be compatible with the PCI-SPECS-master connector, we have fixed the pinout for the I2C bus as shown on fig7.

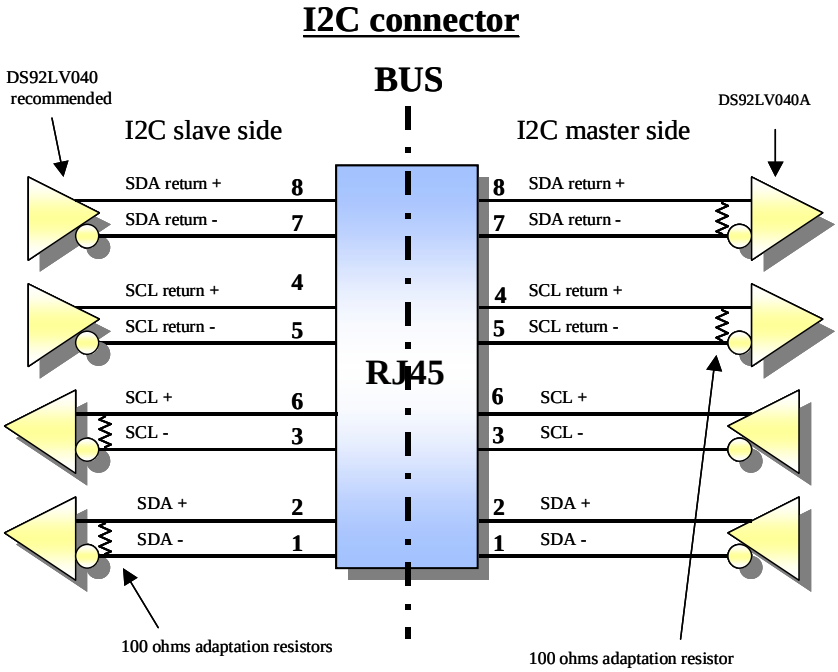


Fig 8 : I2C RJ45 pinout.

5. JTAG bus

The JTAG does not need any specific treatment for long distance bus as I2C. Users only have to implement the adequate bus drivers on the link. Depending on the distance, unipolar or differential drivers may be used. The pinout for the differential remote JTAG bus is shown on fig 8.

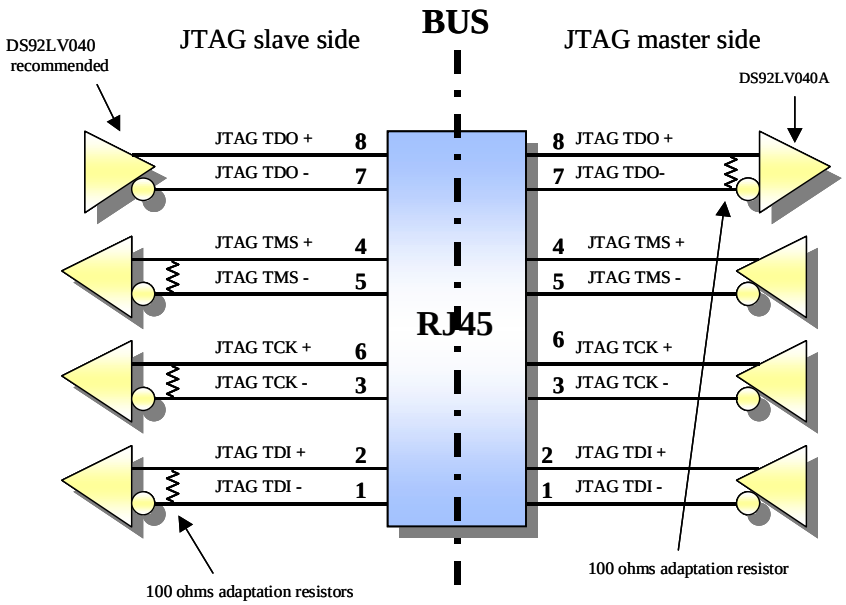


Fig 9 : JTAG RJ45 pinout.

6. Multi-Mezzanine implementation

On the SPECS mezzanine, we provided 2 SPECS interfaces : one point to point for long distance interconnection, one for local bus connection. Thanks to this feature, we can handle several mezzanines on the same SPECS bus. Over a backplane and for short distance, this can be done by interconnecting the lines SDA_BOARD and SCL_BOARD of the different mezzanines (Fig 12). If the number of mezzanines exceeds two, it is mandatory to adapt the bus at both ends. Another important point is to configure the main mezzanine in master mode, this being done thanks to a strap on that board.

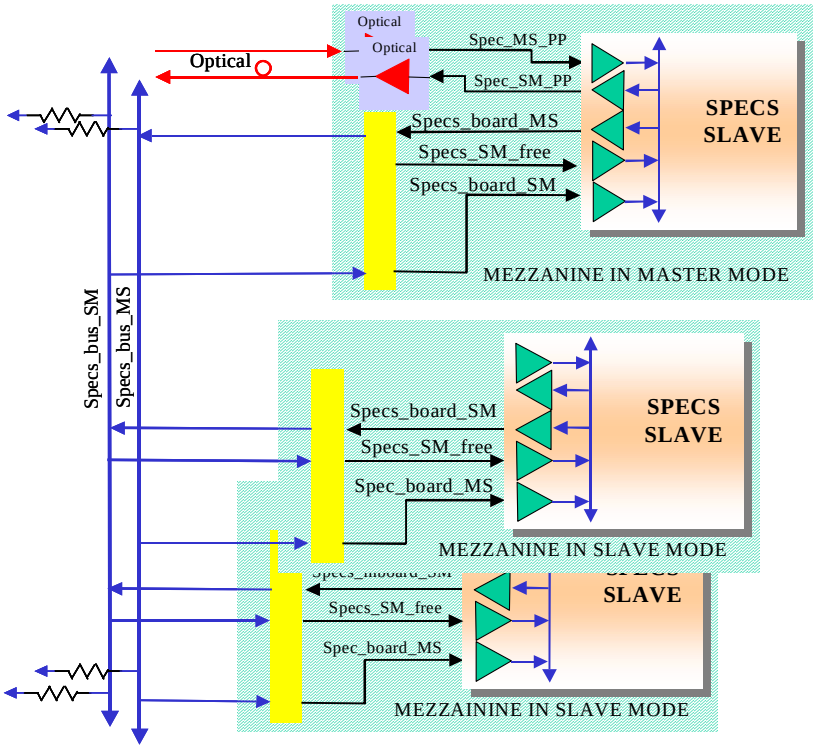


Fig 10 : Multi-mezzanine implementation

This configuration can be applied to a flat cable with the same rules concerning the adaptation.

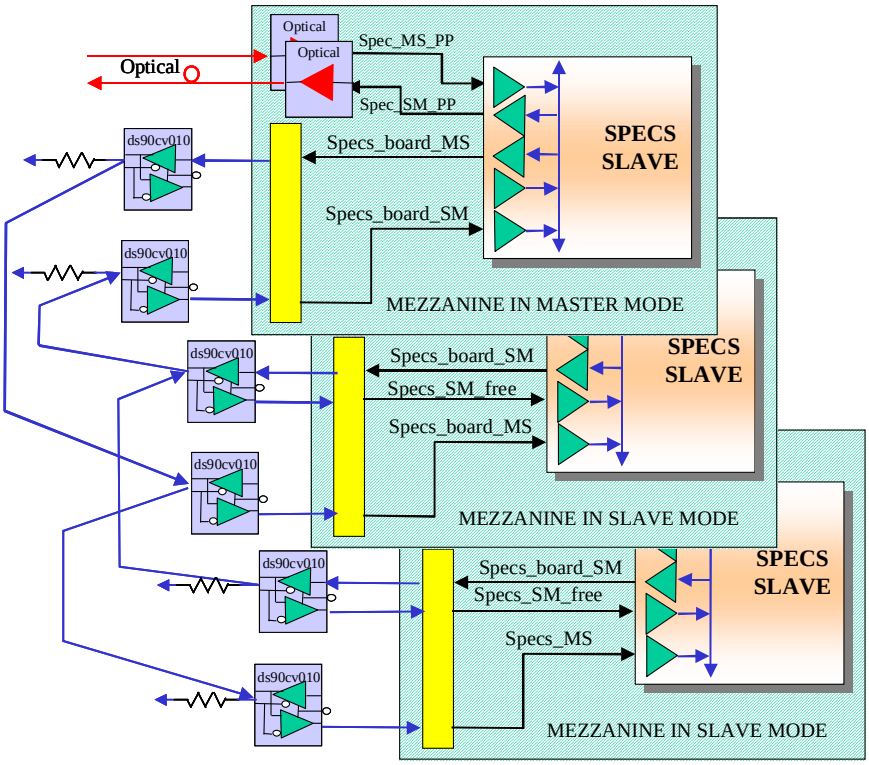


Fig 11 : Multi-mezzanine flat cable application

7. Pinout description

PIN NAME	PIN DESCRIPTION	Levels	Dir	pin number
SDAOUT_BOARD	SPECS bus : SPECS data output data for multi-mezzanine on board (with pull-up at each end of the bus)	LVTTL	O	**JA** 47
SCLOUT_BOARD	SPECS bus : SPECS clock output for multi-mezzanine on board (with pull-up at each end of the bus)	LVTTL	O	**JA** 49
SDAIN_BOARD	SPECS bus : SPECS data input data for multi-mezzanine on board (with pull-up at each end of the bus)	LVTTL	I	**JA** 43
SCLOUT_BOARD_SPY	SPECS bus : for spying the SCLOUT_BOARD line activity	LVTTL	I	**JA** 53
SCLIN_BOARD	SPECS bus : SPECS clock input for multi-mezzanine on board (with pull-up at each end of the bus)	LVTTL	I	**JA** 45
SDA_ I2C_ INT	On-board I2C data bus (with pull-up at each end of the bus)	LCMOS2.5V	I/O/T	**JA** 37
SCL_ I2C_ INT	On-board I2C clock bus (with pull-up at each end of the bus)	LCMOS2.5V	O	**JA** 39
SDA_ I2C	I2C bus : long distance I2C data output	LVTTL	O	**JA** 33
SCL_ I2C	I2C bus : long distance I2C clock output	LVTTL	O	**JA** 35
SDA_ I2CIN	I2C bus : long distance I2C data input	LVTTL	I	**JA** 25
SCL_ I2CIN	I2C bus : long distance I2C data input	LVTTL	I	**JA** 27
RESET_REG*	Reset output. This output does not need any clock to be triggered	LVTTL	O	**JA** 44
USER_INTER	User interrupt. Generates an interrupt towards the SPECS bus	LVTTL	I	**JA** 46
SPARE{3,2,1}	FPGA spare pin	LVTTL	I/O	**JA** 55,52,48
SPARE_con{12,11,10,9}	Spare connector pin.	LVTTL	I/O	**JA** 23,19,17,15
SPECS_CLOCKIN	Clock from motherboard	LVTTL	I	**JA** 26
SPECS_CLOCKOUT	40 MHz mezzanine oscillator. This clock can be disabled through SPECS control register	LVTTL	O	**JA** 22

Table 1 : JA Connector

PIN NAME	PINE DESCRIPTION	Logic	Dir	pin number
TRST_SPECS	For future application	LVTTL	O	**JA** 42
TCK_SPECS	JTAG Bus: Clock JTAG	LVTTL	O	**JA** 32
TDI _SPECS	JTAG Bus: Output data from master JTAG	LVTTL	O	**JA** 34
TDO _SPECS	JTAG Bus: Input data from slave JTAG	LVTTL	I	**JA** 36
TMS _SPECS	JTAG Bus: Command JTAG	LVTTL	O	**JA** 38
CHAN_B [7:0]	Channel_B[7:0] from TTCrx	LVTTL	I	**JA** 67,66,65,64,63,62,57,56
CHAN_B [8]	Channel_A from TTCrx →L0	LVTTL	I	**JA** 68
BU_ID	from TTCrx	LVTTL	O	**JA** 77
L0_EVT	from TTCrx	LVTTL	O	**JA** 78
L0_RST	from TTCrx	LVTTL	O	**JA** 76
L1_RST	from TTCrx	LVTTL	O	**JA** 69
B_CALIB[3:0]	from TTCrx	LVTTL	O	**JA** 75,74,73,72
BUS_R*	Parrallel bus: Read	LVTTL	O	**JA** 83
BUS_W*	Parrallel bus: Write	LVTTL	O	**JA** 84
BUS_DATA[15:0]	Parrallel bus: Data	LVTTL	I/O	**JA** 115,116,113,114,111,112,107,110,105,106,103,104,99,102,97,98
BUS_ADR[7:0]	Parrallel bus: Address	LVTTL	O	**JA** 95,96,93,94,87,92,85,86
DT_RDY	Parrallel bus: Data ready (for slowest component)	LVTTL	I	**JA** 82
DT_ACK	Parrallel bus: Data acknoledge (for slowest component)	LVTTL	O	**JA** 79
VPOS_ANA	5v power supply (For Mezzanine optical version)		I	**JA** 5,9,8,13,14,16
POWER_MEZZANINE	3.3v power supply		I	**J3** 3,4,29,28,59,58,89,88,117,118
GND	Reference gnd		I	**JA** 1,2,11,10,21,20,31,30,41,40,51,50,61,60,71,70,81,80,91,90,101,100,109,108,119,120 7,6,12,18,24,54

Table 2 : JA Connector

PIN NAME	PIN DESCRIPTION	Level	Dir	Pin number
REG_EXT31:0]	User defined control/status register. Every I/O can be configured as input or output through a SPECS control register. This register does not need any clock to be written	LVTTL	I/O	**JB** 116,115,114,113,112,109,108,107,106,105,104,103,102,99,98,97,96,95,94,93,92,87,86,85,84,83,82,79,78,77,76,75
I2CJTAG_DE[15:0]	I2C & JTAG bus : controls the direction for the external bus drivers	LVTTL	O	**JB**: 74,72,68,66,64,62,56,54,52,48,46,44,42,38,36,34
I2CJTAG_RE[15:0]	I2C & JTAG bus : controls the selection for the external bus drivers	LVTTL	O	**JB**: 73,69,67,65,63,57,55,53,49,47,45,43,39,37,35,33
I2C_ADDRESS[6:3]	I2C Address for on-board ADC	LCMOS2.5V	I	**JB** 18,16,14,12
SPARE{3,2,1,0}	Spare connector pin.	LVTTL	I/O	**JB** 26,32,,23,25
InAn[5:0]	Analog input channel (max dynamic range 1.75v)	Analog	I	**JB** 6,8,5,7,9,13
iout10		Analog		**JB** 17
External resistor	Input for thermal sensor	Analog	I	**JB** 22
POWER_MEZZANINE	3.3V Power supply		I	**JB** 3,4,29,28,59,58,89,88,117,118
GND	Reference gnd		I	**JB** 1,2,11,10,21,20,31,30,41,40,51,50,61,60,71,70,81,80,91,90,101,100, ,111,110,119,120 15,19, 27, 24

Table 3 : JB connector

PIN NAME	PIN DESCRIPTION	Logic	Dir	pin number
SDA_MS	SPECS Bus : data from master +/-	LVDS	I	**RJ45** 2/1
SCL_MS	SPECS Bus : clock from master +/-	LVDS	I	**RJ45** 6/3
SDA_SM	SPECS Bus : data from slave +/-	LVDS	O	**RJ45** 8/7
SCL_SM	SPECS Bus : clock from slave +/-	LVDS	O	**RJ45** 5/4

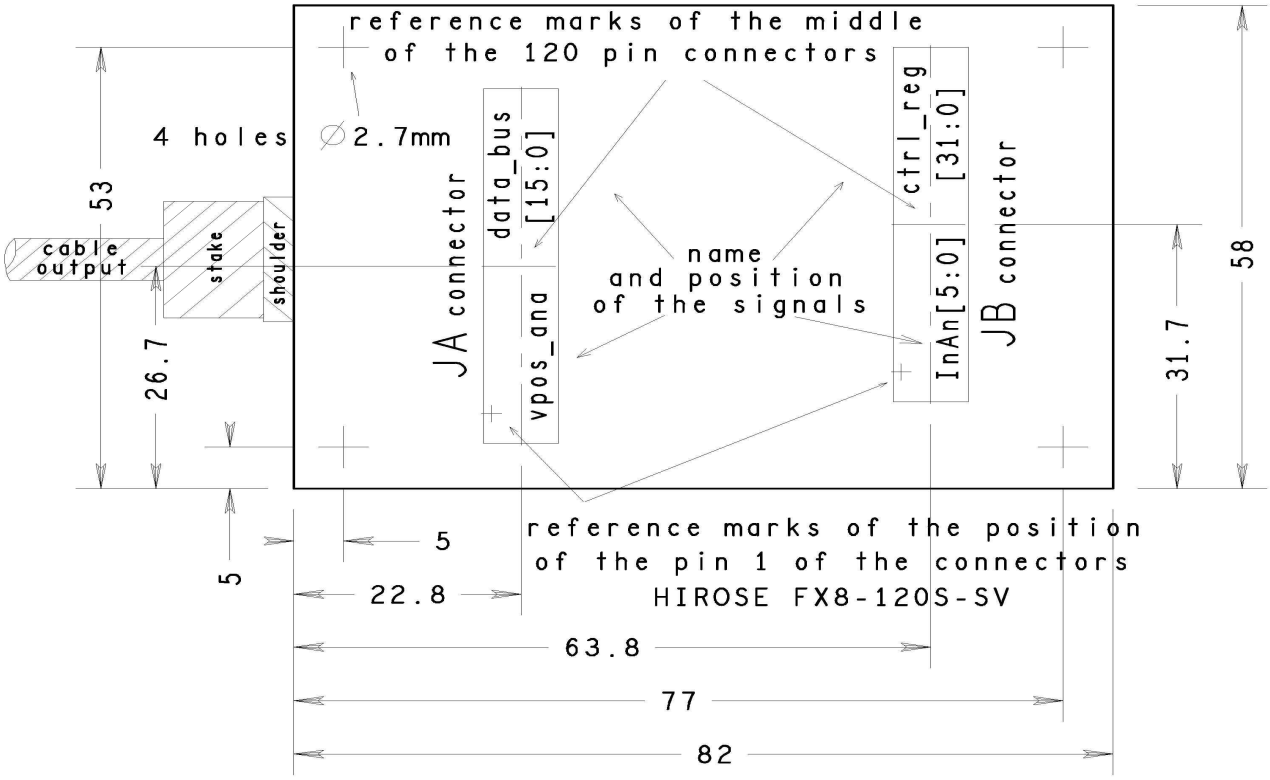
Table 4 : RJ45 connector

Mother-board JA& JB connector:reference: HIROSE FX8-120S-SV (stacking height 3.2mm)

Web documentation on www.hirose.com

8. Physical Dimensions

Drawing of the outline and of the female connectors on the motherboard



9. Command register

The register access was done by a C libraries, the specific documentation is provide with the SPECS master software.

Mode		Register	Parameters
3	**REGISTER** Wr (16 bits) Rd (16 bits)		Reg_Data [15:0] = 2 x SPECS data [7:0]
3	External ctrl/status register Configuration ctrl/status register	**Reg_out**[31:0] Rd/Wr **Conf_regout** [31:0] Rd/Wr	data [7:0] @ Sub_address [7:0] = 0 data [15:8] @ Sub_address [7:0] = 1 data [7:0] @ Sub_address [7:0] = 2 data [15:8] @ Sub_address [7:0] = 3
3	Mezzanine ctrl/status	**Mezz_ctrl** [7:0] {osc,Mas/Sla,//bus_conf,rst_reg} Wr/Rd **Mezz_stat** [7:0] {to be defined} Rd	data [7:0] @ Sub_address [7:0] = 4 data [15:8] @ Sub_address [7:0] = 5
3	Interruptions : Interrupt_vector IT_Configuration_vector	**Interrupt** [10:0] {Interrupt_Vector [7:0], User_interrupt, Header_checksum, Trailer_checksum} (Rd) **IT_Config_vect** [7:0] Rd/Wr	data [10:0] @ Sub_address [7:0] = 6 data [7:0] @ Sub_address [7:0] = 7
3	Identification + Board_number -> register 1 Serial_number + Revision_number -> register 2 User_defined -> register 3	**Board_ID** [15:0] {Identification [7:0], board_nb [7:0],} Rd **Ser_Rev** [15:0] {serial_nb [7:0], revision_nb [7:0]} Rd **Userdef_test** [15:0] Rd/Wr {user_defined [7:0], test [15:8] }	data [15:0] Sub_adress [7:0] = 8 data [15:0] Sub_adress [7:0] = 9 data [15:0] Sub_adress [7:0] = 9

Mode		Controlled I/O	Parameters
0	**I2C**	SDA SCL	I2C data [7:0] = SPECS data [7:0]
1	**JTAG**	TDO TDI TCK TMS (TRST INT)	JTAG data = SPECS data
2	**PARALLEL BUS**	DATA ADDR RD + WR	data [15:0] = 2 x SPECS data [7:0]

10. References

[1] Serial Protocol for the Experiment Control System of LHCb, Version 2.0, D.Breton and D.Charlet, LHCb note 2003-004.

[2] Powerpoint presentation of D.Charlet about the common calorimeter backplane at the calorimeter electronics review, July 2002, http://doc.cern.ch/AGE/current/askArchive.php?a02959/a02959s1t3/transparencies/Charlet.pdf.

[3] LHCb-2002-072: Single event effects and actel AX FPGA, Machefert, F

[4] LHCb-2002-021: LHCb calorimeter front-end electronics radiation dose and single event effects, Beigbeder, C; Breton, D; Charlet, D; Lefrançois, J; Machefert, F; Tocut, V; Truong, K