DAQ Hardware Components

LHCb Online Meeting

15 June 1998

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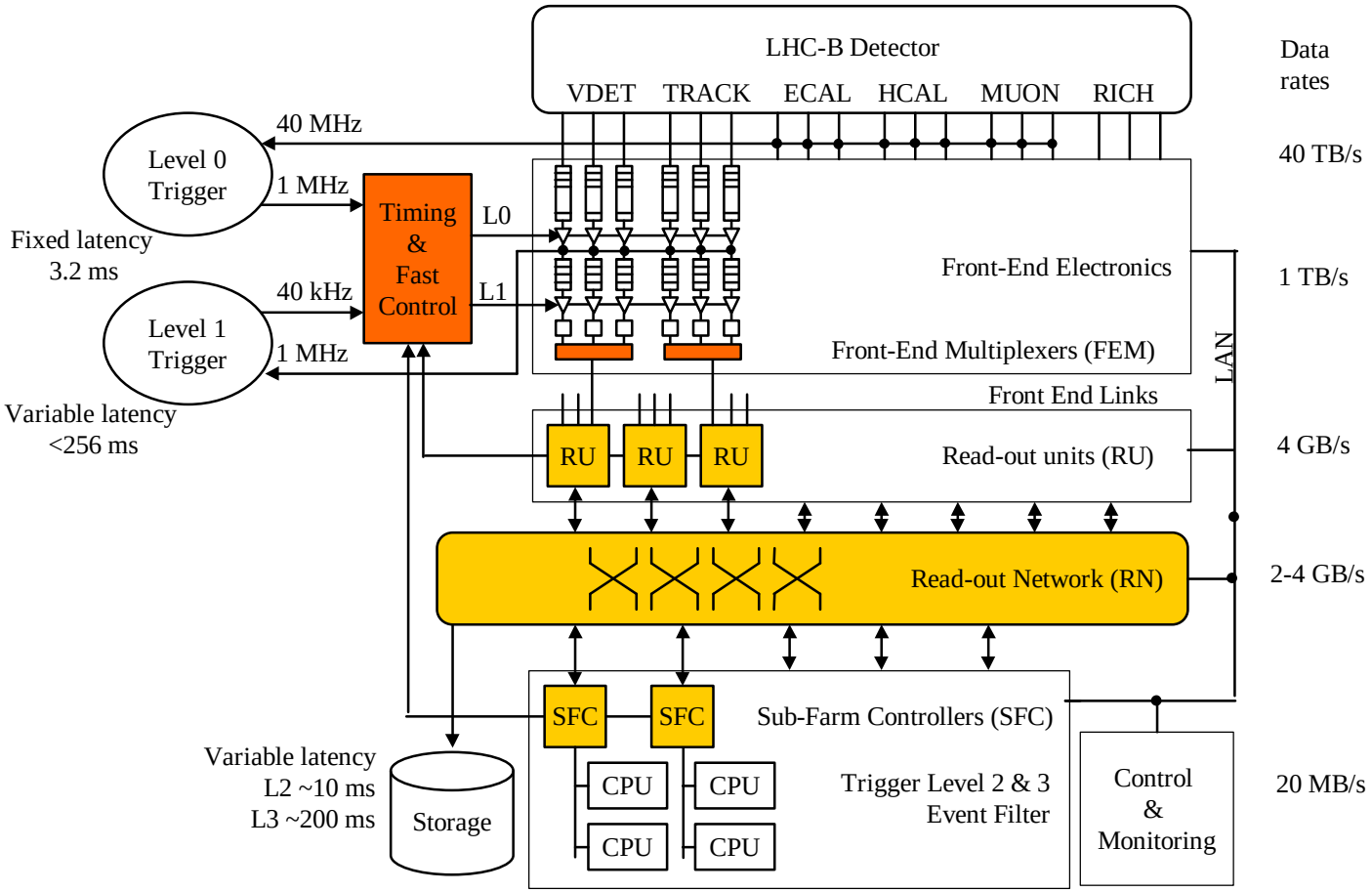
General Architecture



Timing & Fast Control

- Provides the interface between the Trigger System, the Front-End Electronics and the Readout System
- It has to drive the TTCtx
- It has to implement the "global" rules to prevent buffer overflows like
  - not more than x L0Yes in n microseconds (for L0 de-randomizer)
  - not more than y L0Yes in m microseconds (for L1 buffer)
  - perhaps no 2 L0Yes in consecutive bunch crossings
  - ...
- It will implement a control port that allows to set it up and monitor its performance
- It will provide data to the DAQ

Front-End Multiplexer

- So far the policy was that the DAQ starts at the output stage of the FEM
- However, under the assumption that between the zero suppression and the filter farm no detector specific processing is necessary, it s quite obvious that the functionality is the same everywhere and hence a common approach should be aimed for.
- The task of the FEM is to perform a multiplexing of ~2000:100 @ 40 kHz nominal rate.
- The input data is variable length and arriving asynchronously. In this sense the FEM functionality has very much in common with the RU in the full readout protocol.

Read Unit

- The Readout Unit (RU) multiplexes the data from 1 to 3 front-end links onto one link of the readout network
- In it s output stage in implements the source part of the event building protocol.
- It has to have sufficient buffering to cope with fluctuations in the data flow and the latency of the trigger throttle in case the internal buffer gets full.
- In the case of the phased readout protocol it also has to provide buffer space during the Level-2 latency

Readout Network

- The readout network has to provide the necessary bandwidth and connectivity to perform the event building task under the given conditions of event size and trigger rate
- It also has to support the necessary communication paths for the chosen event building protocol

Sub-farm Controller

- The sub-farm controller implements the receiving end of the event building protocol at its input stage
- It is responsible for transmitting a built event to one of the CPUs attached to it
- Events accepted by Level-2 and 3 will be transferred from the CPUs via the SFCs through the readout network to storage
- Load balancing between the CPUs on a sub-farm is aso the responsibility of the SFC
- The SFC can throttle the trigger and has to provide sufficient buffering to cope with the throttle latency

Event Filter Farm

- The Event Filter Farm has to provide sufficient CPU power to run the Level-2/3 trigger algorithms
- There is an Event filter joint project between the LHC experiments and IT to study the management issues of filter farms and the dataflow in and out of the farms.

Summary

- Some components are being worked on (RU,Event building)
- However some components need effort in near future
  - Timing and Fast Control (in collaboration with detector groups)
  - Front-End Multiplexers (if not implemented using RUs)
- Before building the full system for LHCb all components need to be integrated in a "String Test" (vertical slice)