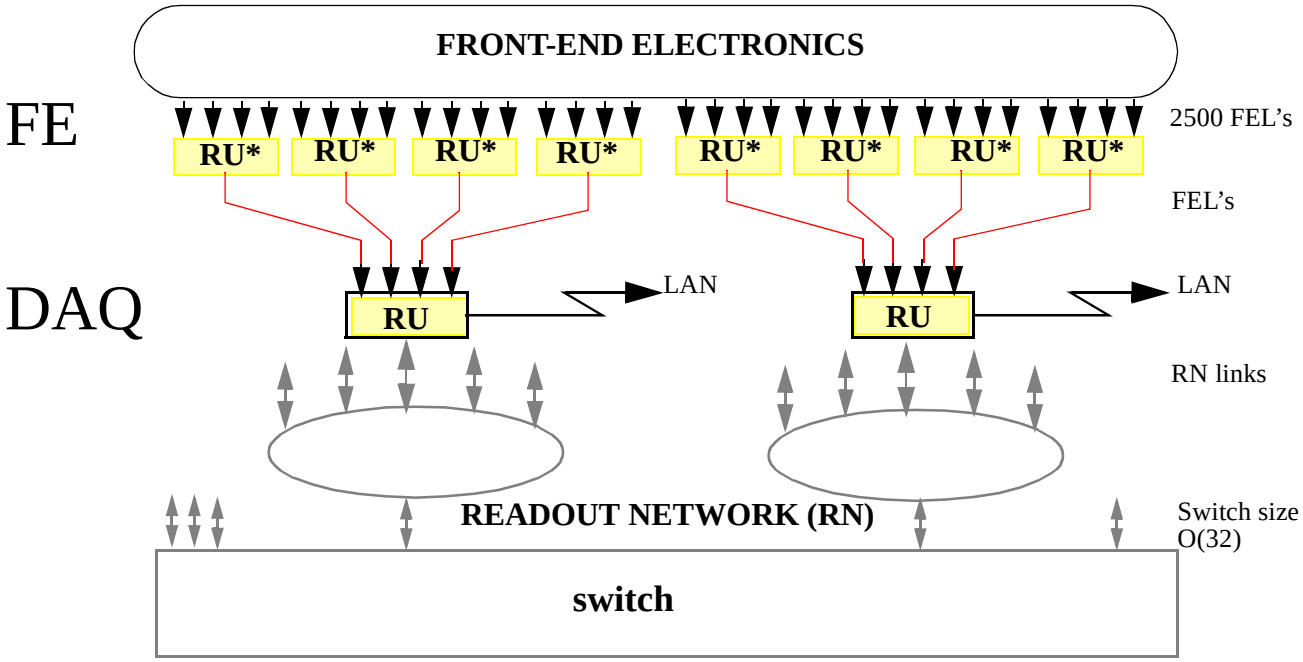
READOUT UNIT

Application A: DAQ and MUX (option)



* only SEM functionality of RU in use

Figure 1: Extended use of RU between ODE and RN

Table 1: RU design parameters (DAQ EB interface)

Parameter	RU
Frontend link inputs	up to four S-link Gbit receiver mezzanines
PCI output(s) for RN interface cards	One 64 bit, 66 MHz PCI port (PMC) One 32 bit, 33 MHz PCI port (PMC)
Gbit link multiplexing	four S-link cards, 40 Mbyte/s each (nominal)
SEB subevent event buffer	1 MByte DPM, upgradable 10 Mbyte max.
Integral input bandwidth (nominal)	160 MByte/s
Peak bandwidth per link input	80 Mbyte/s
Throughput (nominal)	~160 MByte/s
Raw bandwidth	~256 Mbyte/s
Input link technology	32 bit S-Link simplex (optionally: duplex)
Output link technology	all technologies complying with PCI bus Rev. 2.1
Remote control and monitoring	10/100-BASE-TX port with an RJ45
Eventbuilding protocols	LHCb full readout & phased readout

Application B: Vertex trigger (IHEP)

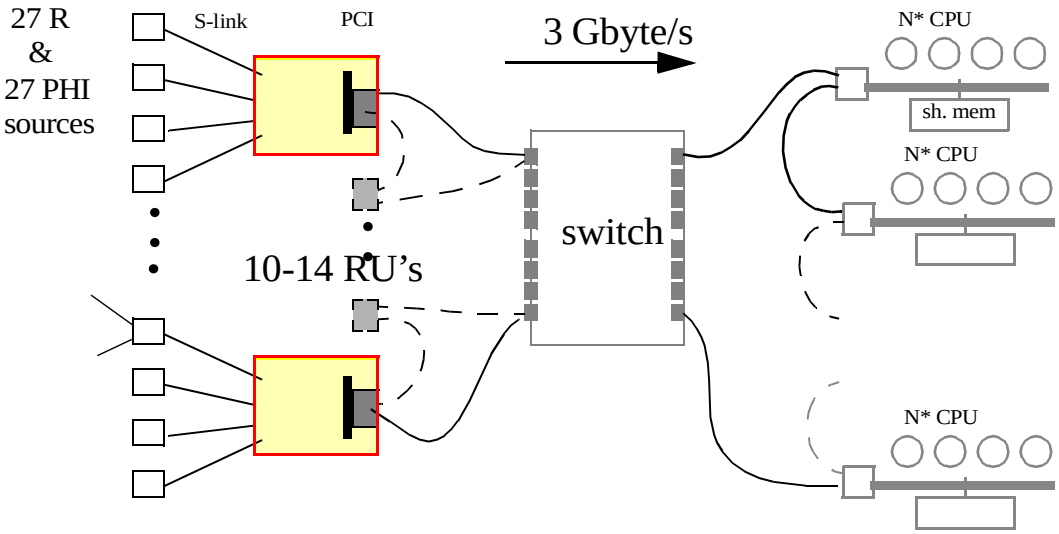


Figure 2: Application example: Vertex Level-1 data

Table 2: RU requirements (Level-1 Vx multiplexer)

Parameter	RU
Frontend link inputs	up to four S-link Gbit receiver mezzanines with up to four individual receivers
PCI outputs for shared memory interface card and TTCrx timing synchronization card	One 64 bit, 66 MHz IEEE P1386 (PMC) one 32 bit, 33 Mhz (PMC)
Gbit link multiplexing	four S-link cards, 40 Mbyte/s each nominally
SEB subevent event buffer	1 MByte DPM, upgradable 10 Mbyte max.
Integral input bandwidth (nominal)	240 MByte/s
Peak bandwidth per link input	80 Mbyte/s
Throughput (nominal)[a]	~256 MByte/s
Raw bandwidth	~512 Mbyte/s[b]
Input link technology	32 bit S-Link simplex (optionally: duplex)
Output link technology	all technologies complying with PCI bus Rev. 2.1
Remote control and monitoring	10/100BASE-TX port with an RJ45
Eventbuilding protocols	shared memory

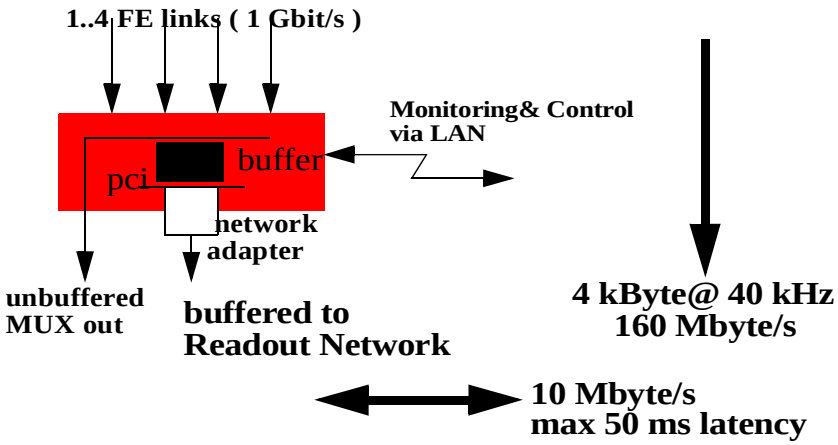
a.multiplexing factor of four
b.technology of PCI 64 @ 66 MHz

RU Global requirement

FE Link data size@ 40 kHz [bytes]

Vertex	240 byte
i.Tracker	230
o.Traccker	600
rich 1	690
rich 2	250
preshower	330
ecal	500
hcal	500
muon	125
trigger	500

derived from: TP.



Blocks and terms

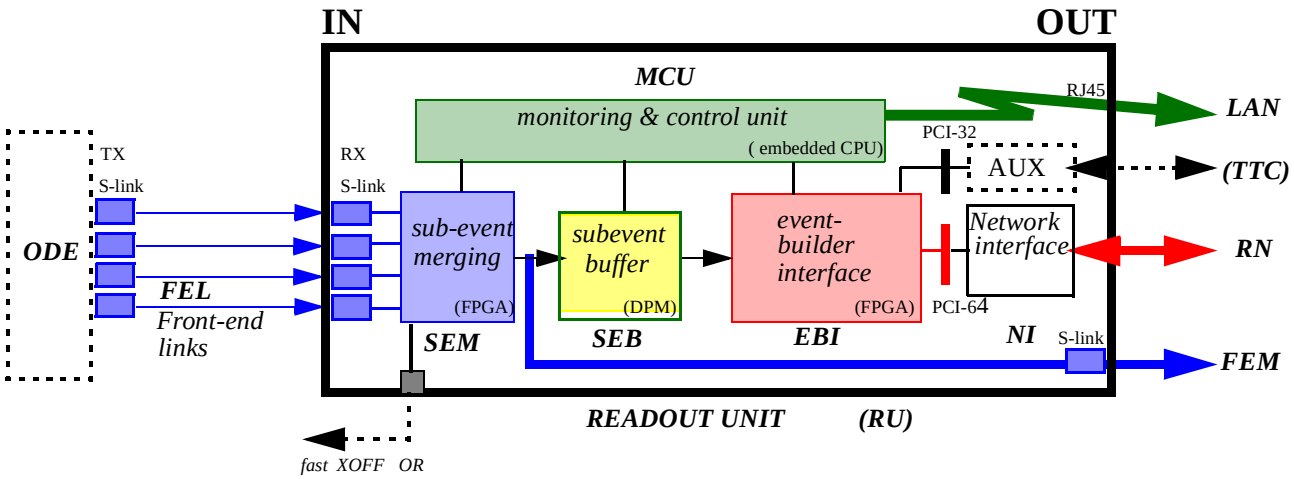


Figure 3: Overview Readout Unit

The EP-ED team

- **Frontend Links, RU receiver logic .....Francois Bal**
- **SEM and EBI (VHDL), data scheme .....Jose Toledo (doct. student)**
- **Cadence and layout ....L.Mcculloch (unforeseen illness leave !!!)**
- **MCU low level software .....E.Watson**
- **Remote control ....B.Bruder (cooperant as from Sept. 99)**
- **Documentation, decisions, coordination .....H.Muller**

RU Architecture

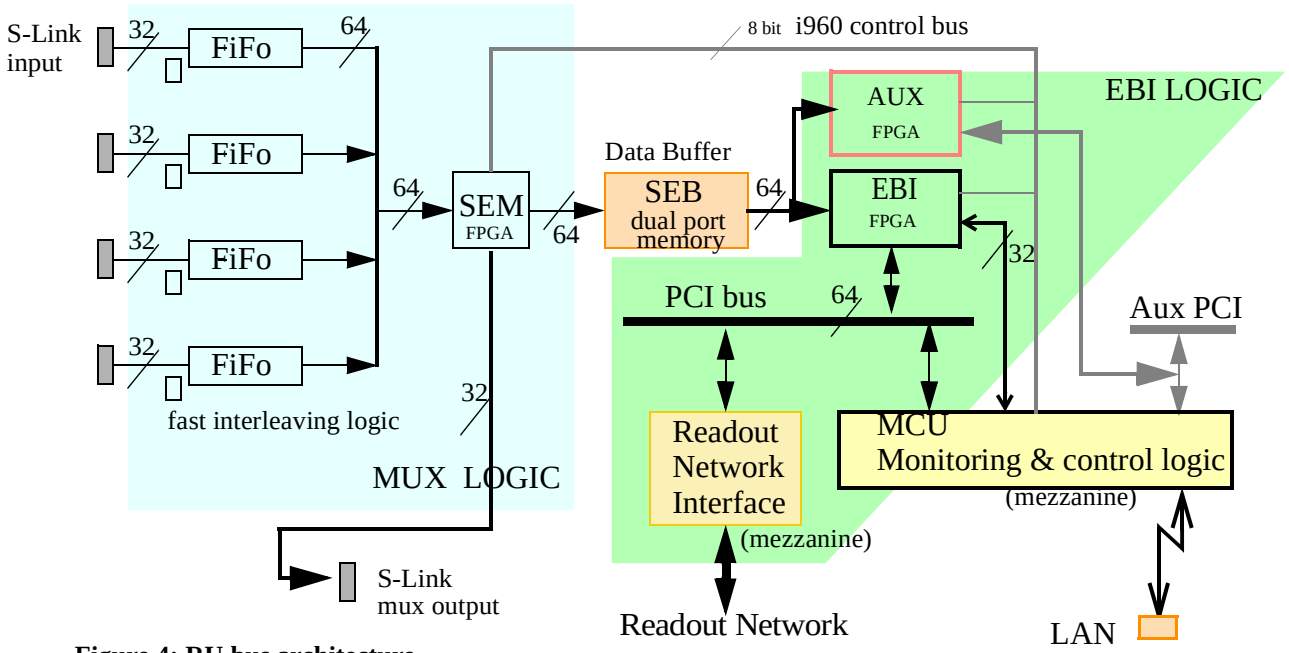


Figure 4: RU bus architecture

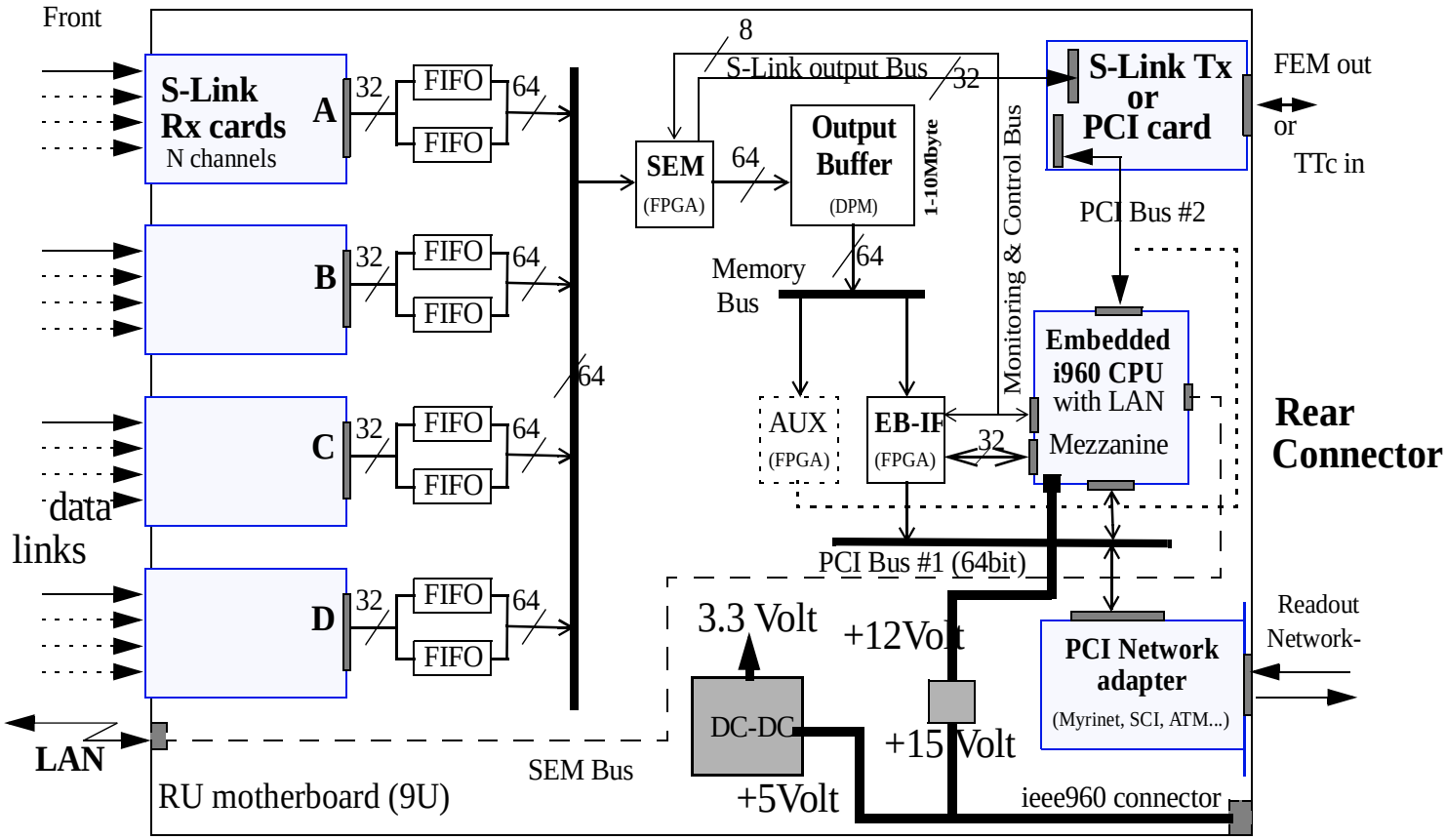
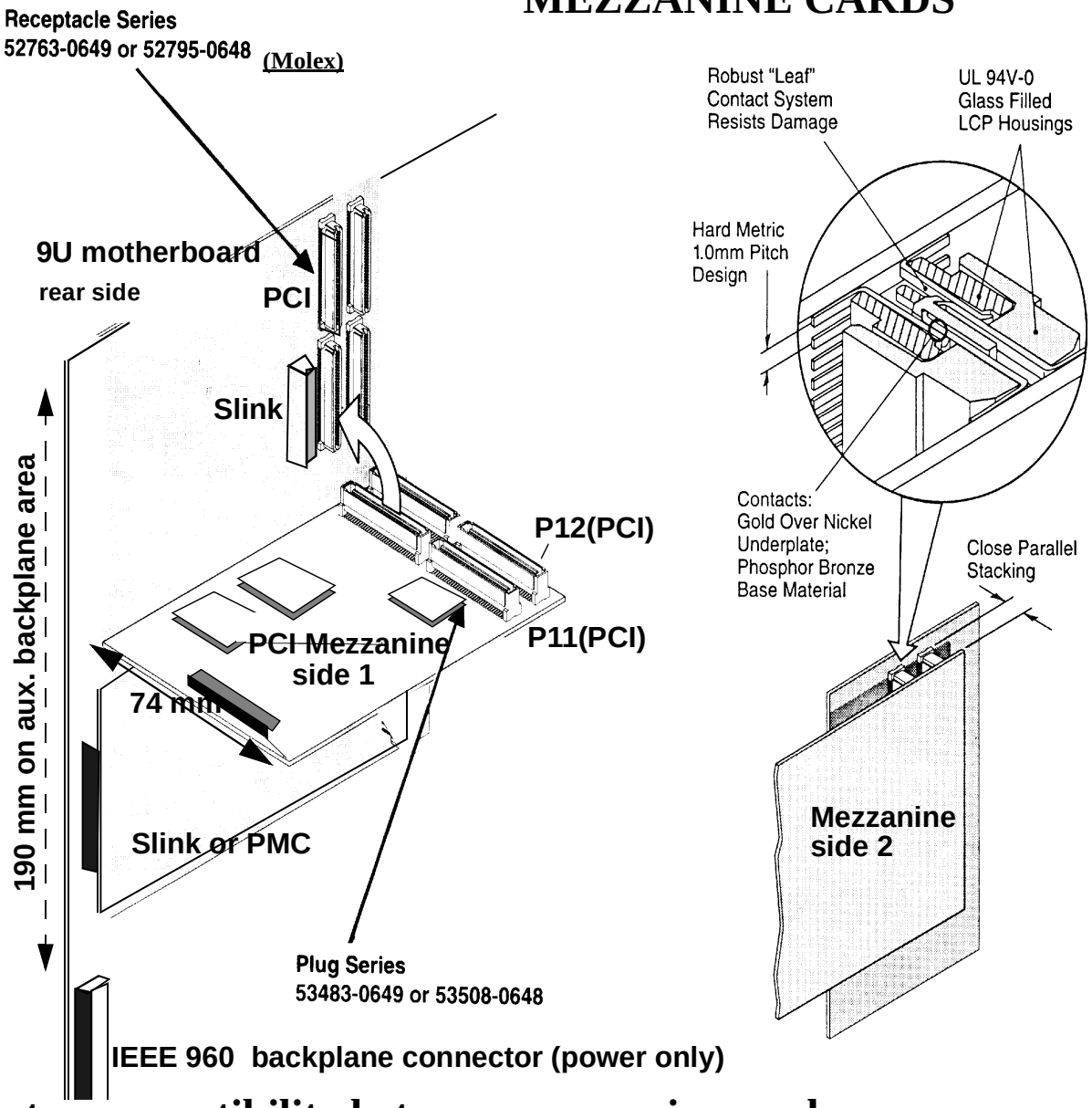


Figure 5: Prototype 9U motherboard

MEZZANINE CARDS



Connector compatibility between mezzanine cards

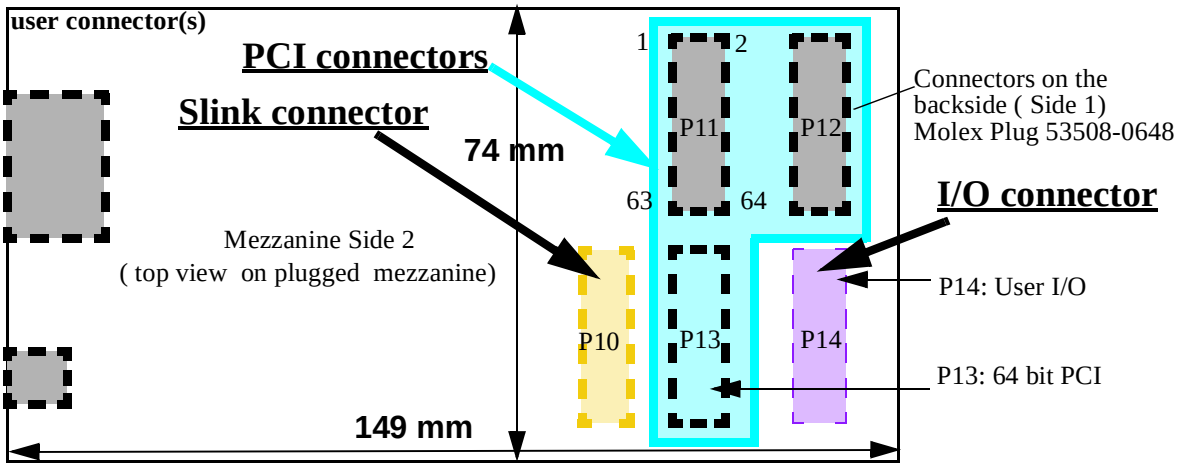


Figure 6: PMC and Sbus mezzanines in IEEE P1386.1 (PMC) formfactor

Mezzanine stackheights (PMC and Slink)

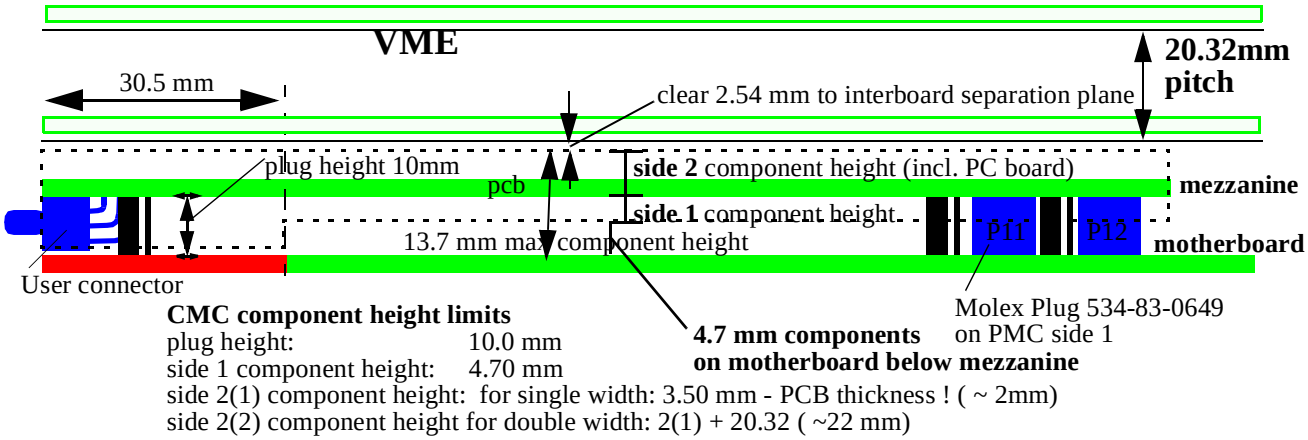


Figure 7: Slink and PMC mezzanine mechanical constraints for standard VMEbus

- Use of IEEE960 mechanics for prototype

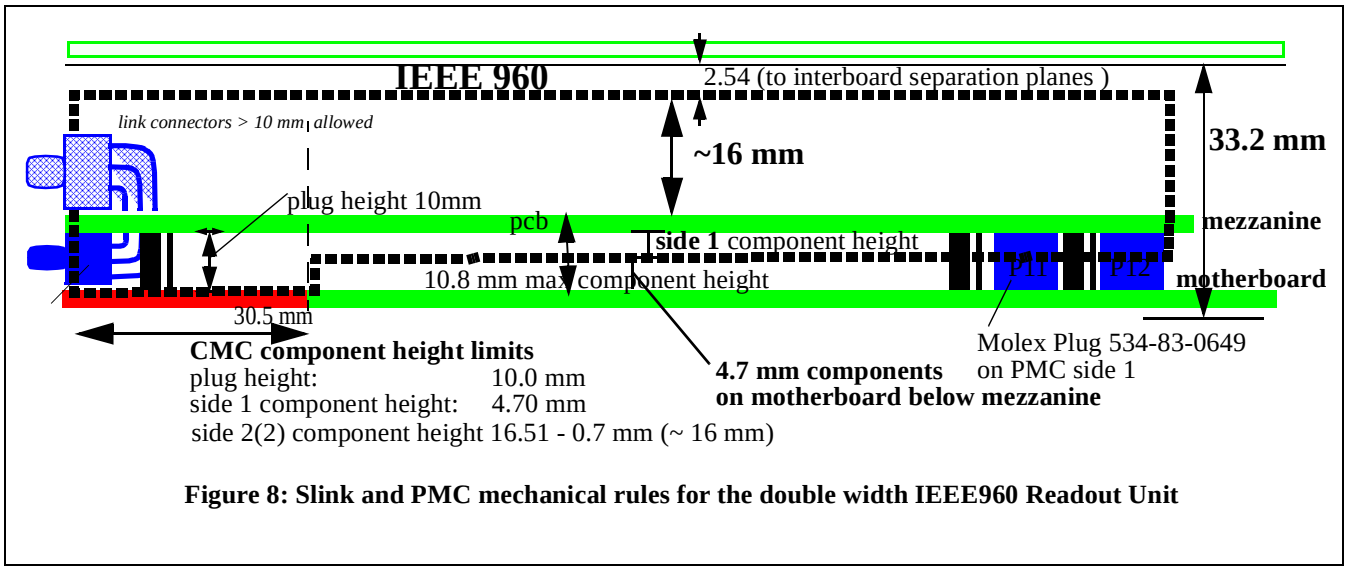


Figure 8: Slink and PMC mechanical rules for the double width IEEE960 Readout Unit

IEEE960 mechanics Pro's:

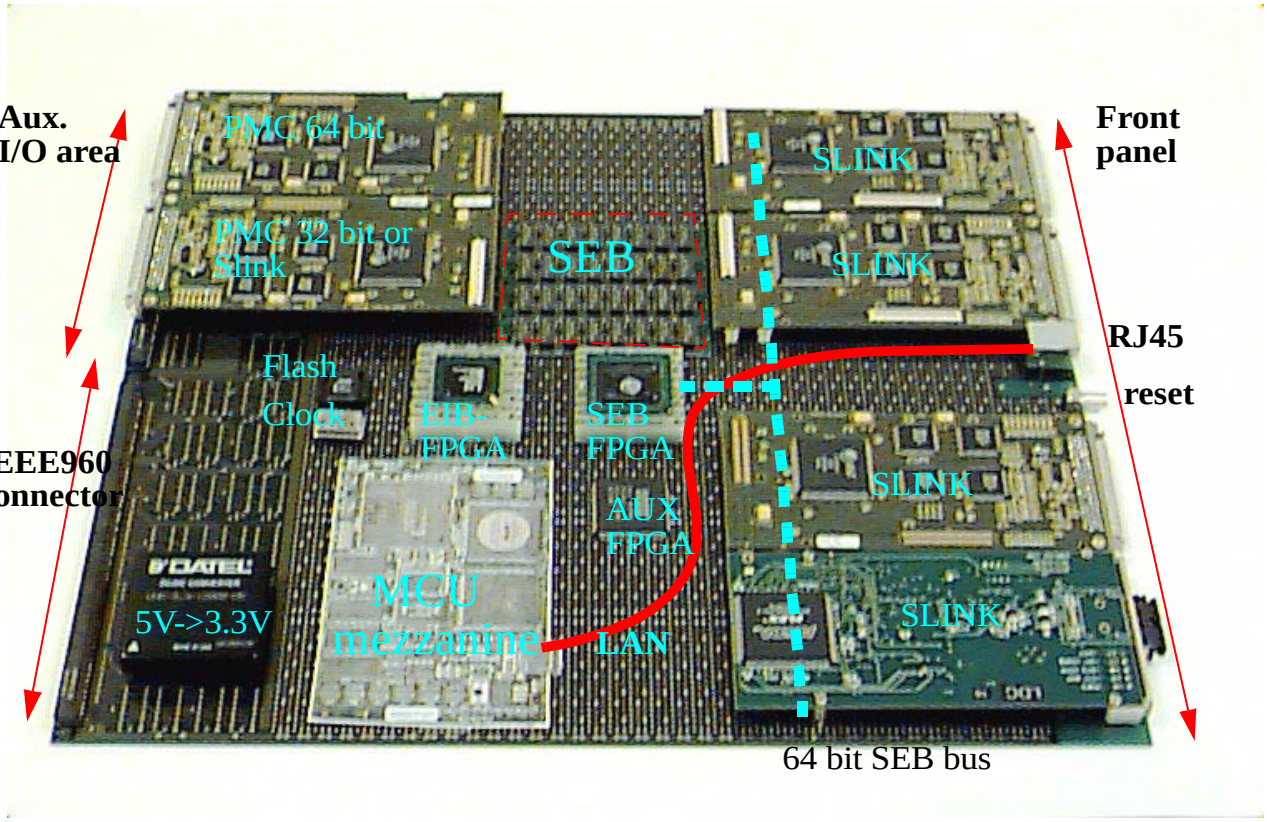
- **6 PMC's**
- **13 dual-width modules/bin, up 10Watt per PMC,**
- **existing 9U bins in watercooled racks in PA8**
- **enough power (85 Watt/RU).**

Table 3: 85 Watt RU power consumption details

	P1386 Mezznines PMC / Slink	FiFos IDT 72V3660L15PF	MCU mezzanine PXEcore	Dual Port memories IDT70V927 9S12PRF	FPGA Lucent OR3Txx	Glue logic: Pals, clock, timer, Flash
Consumption per component [W]	**7.5** (single height) **12** (dual IEE960) interpolated: **10**	250 mA @ 3.3V * (1/2) = **0.4**	600 mA @ 12 Volt= **7.2**	200 mA * 3.3 Volt= **0.6**	SEM : **2** AUX: **2** IEB: **1.5**	**5**
Max. Nr. o.Com-ponents	6	8	1	8	3	<10
totals	**60**	**3.2**	**7.2**	**4.8**	**5.5**	**5**

Total = 85 Watt

) Artistic view of 9U RU prototype board



- **9U IEEE-960 card (similar components like planned)**
- **Four S-link mezzanine cards for 2W -front panel**
- **Two PCI/Slink cards on rear (1/2 cardheight empty)**
- **A double width frontpanel (33 mm): 13RU modules per bin**
- **The DC-DC converter up to 12 A of 3.3 Volt supply from 5 Volt**
- **IEEE 960 rear connector merely used for power**
- **Embedded CPU (optional) plug-in card with LAN**

Table 4: RU full bin power requirement

power modules	Maximum current	No of modules needed
+5 V	100 A	2
+15 V	25 A, 30 A	1

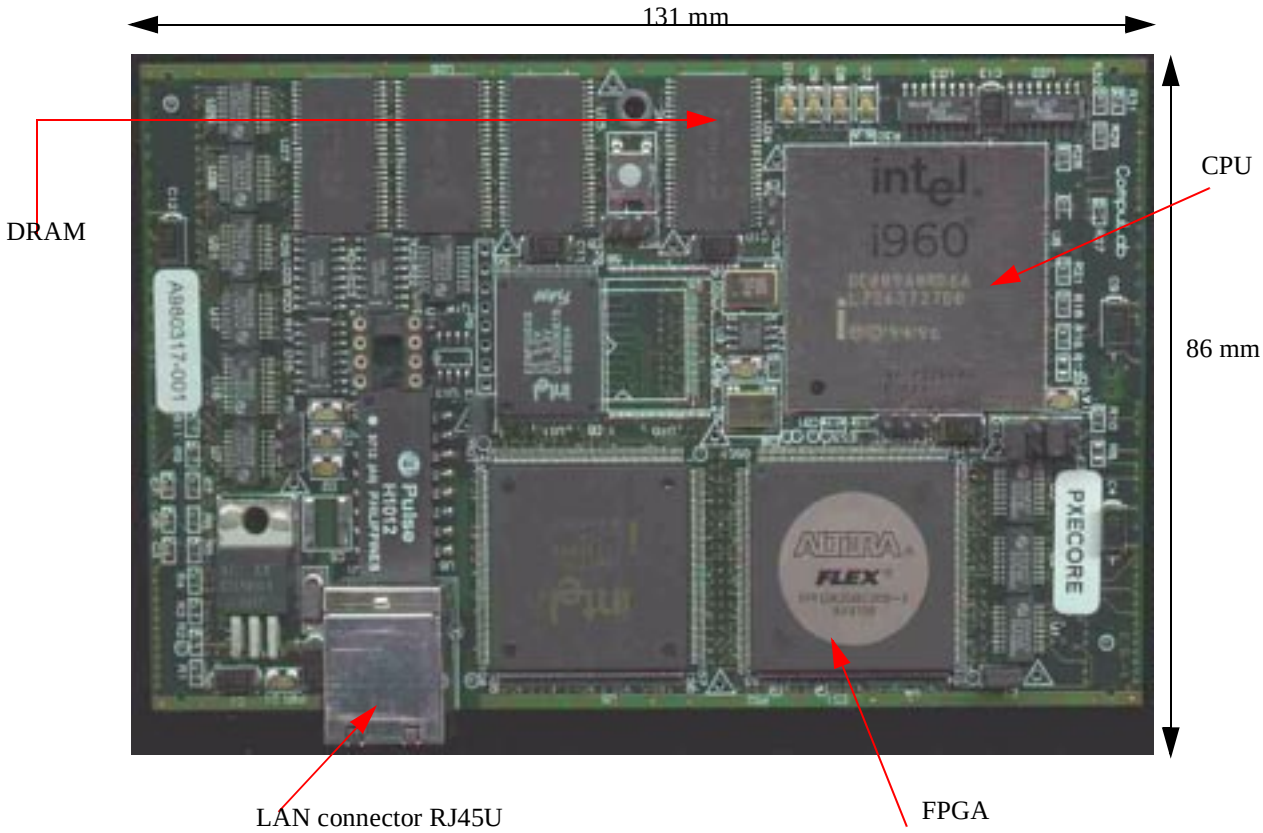


Figure 9: Photo of MCU mezzanine card

100 MHz Intel 80960RD RISC, 10/100 Ethernet controller, embedded Flash EPROM and I/O FPGA

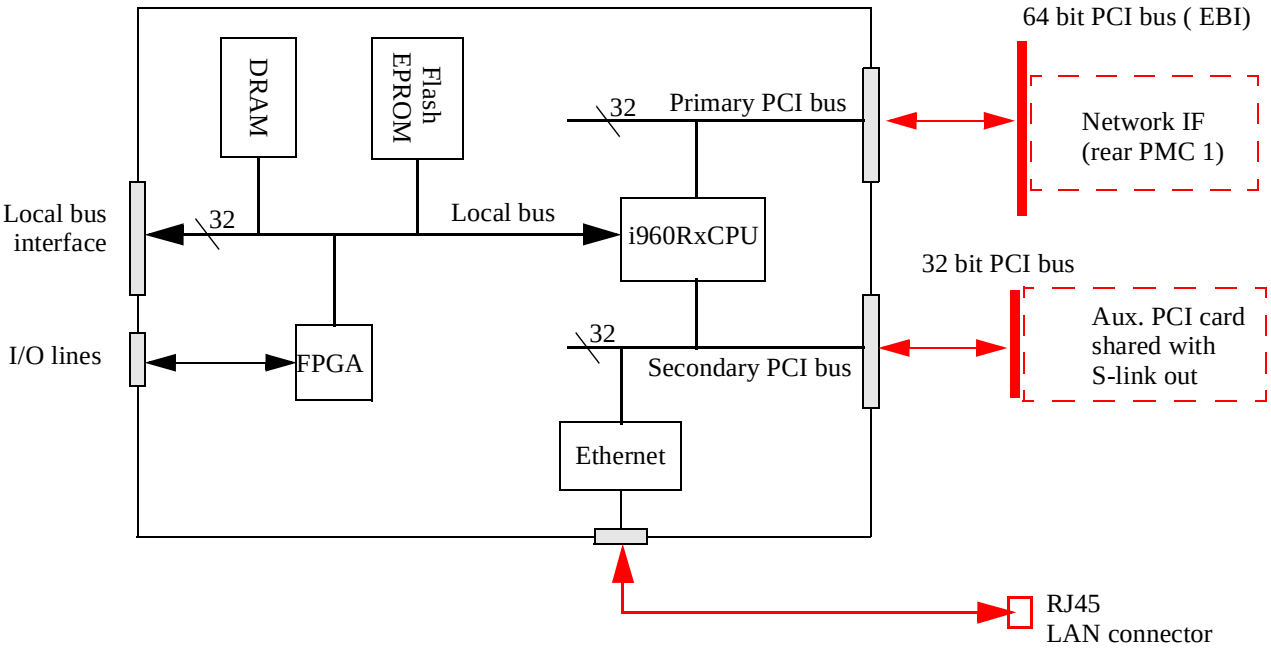
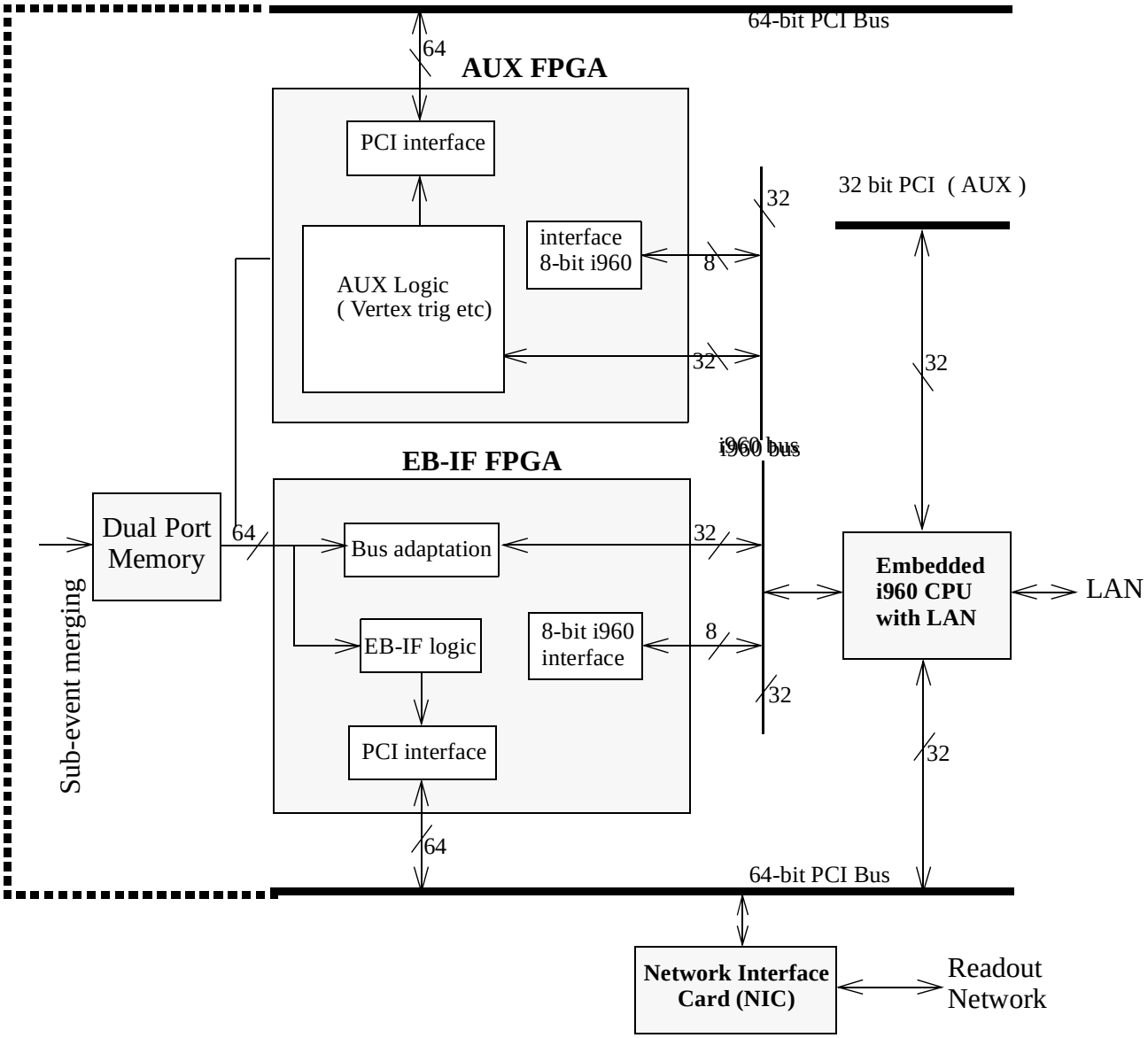


Figure 10: MCU module architecture

RU output stage



Data Formats

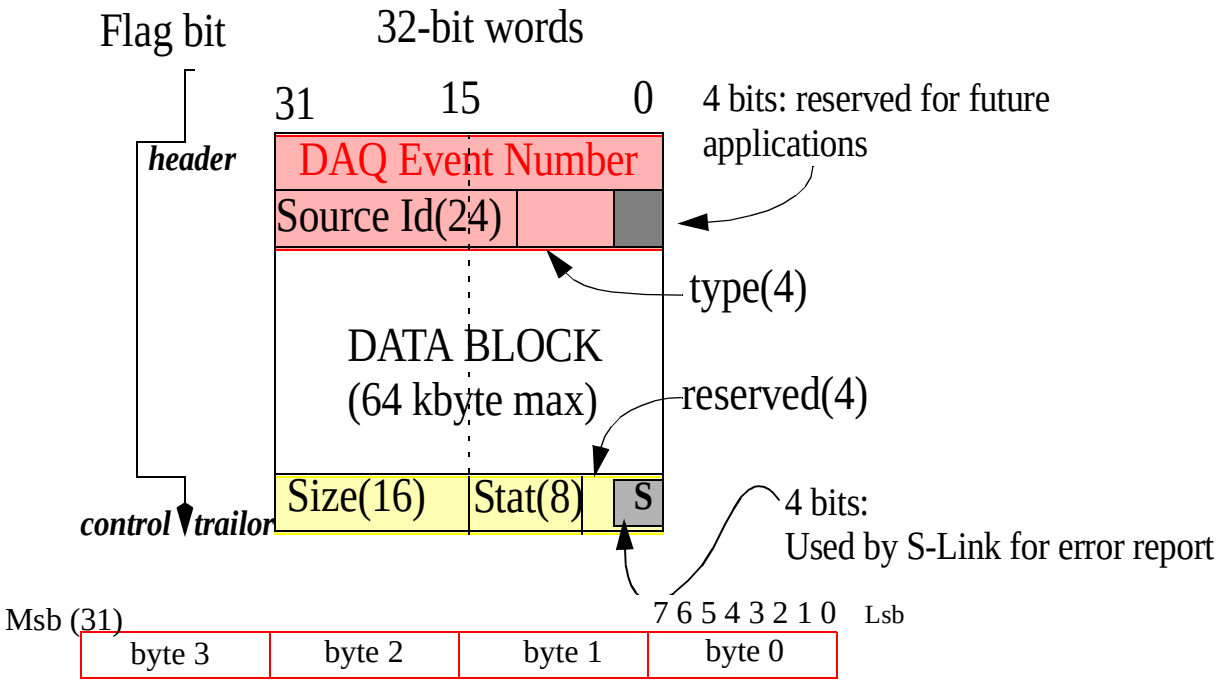
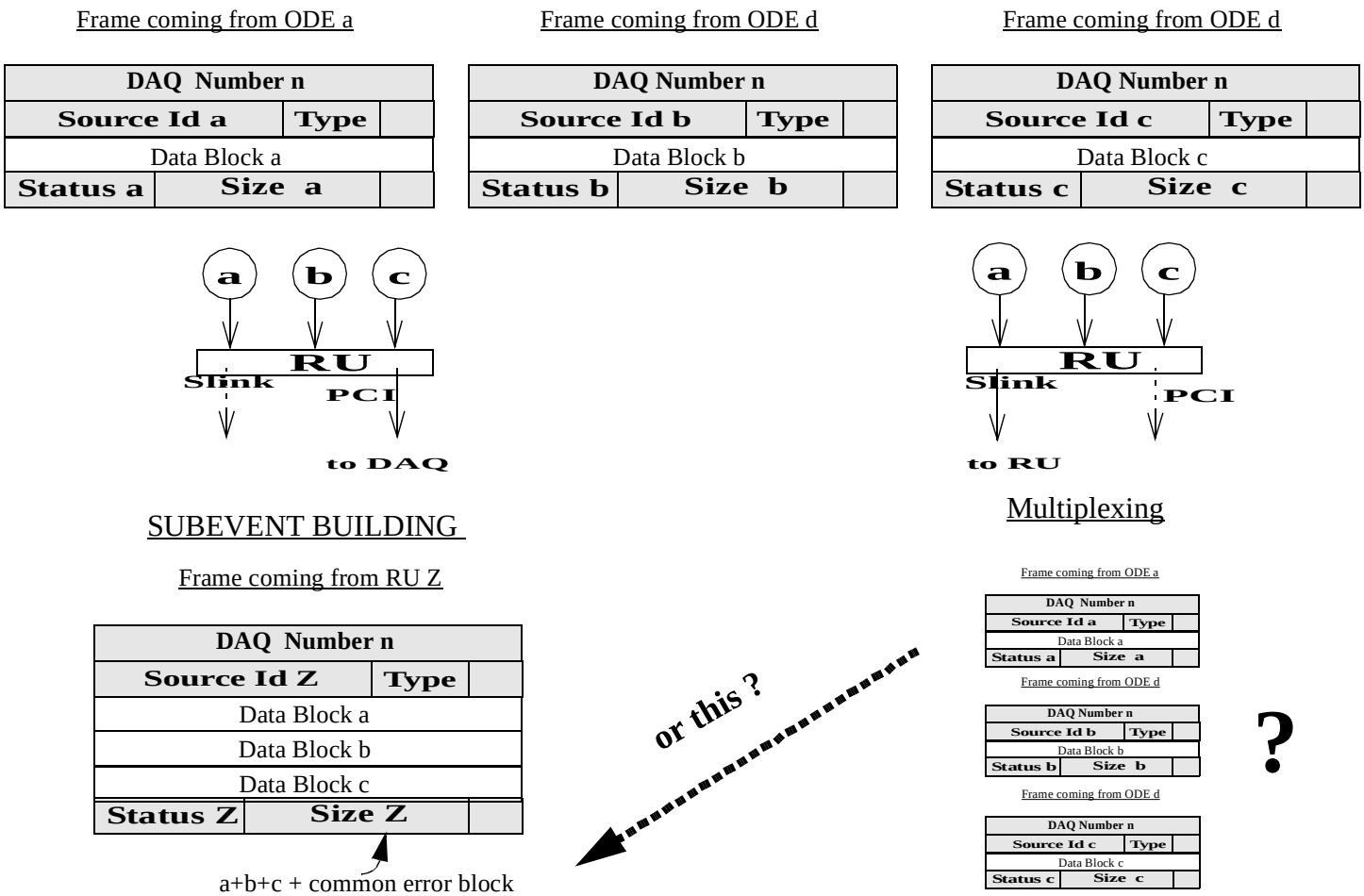


Figure 11: little endian byte ordering (Intel)

SUBEVENT Building/Multiplexing



Questions arising from this meeting:

Q: !60 Mbyte throughput, why ? A: 4 links with 1 kByte incl. overhead @ 40 kHz

Q: Multiplexing option, why ? A: the input stage of the RU is a multiplexer, see architecture RU

Q: IHEP application requires 4 * more RU's than shown..

A: If each R,PHI station has 2 (or 4) sources, these can get merged togehther via one S-link receiver, so No of RU's stays 10-14

Q: Why is the requirement for the Vertex 240 Mbyte/s

A: 3 Gbyte/s divided by 14 plus some 10% overhead.

Q: Is the IHEP requirement justified: added complexity to enhance the RU via the use of a second FPGA

A: No added complexity nor cost, an option to place another FPGA on the board. Also, the RU application may need this FPGA as well to achieve more than 256 Mbyte/s on the output PCI bus (two PCI masters in parallel)

Q: Is the timescale, i.e. protoboard till end summer still valid ?

A: We have delays of at least 2-3 month since our Cadence engineer had to go on an immediate illness leave for 2 month

Q: the multiplexing as shown here(concatenation over a single output) is not what the DAQ thinks, it should reduce the numbers of packets ?

A: We can do this however we better chexk with the FE groupes what they understand under multiplexing when using for example VME. Concatenation of individual input packets or building of a merged packet with new wordcount and status

Q: the slow controls issue you plan to look into using the mebedded CPU with a cooperant, maybe we should make this part of a larger activity to understand DCS.

A: We will start for zero in September when the Cooperant arrives, and we plan to compile all the RU requirements

Q: maybe we should alos look into alternatives for a simple and fast Xon/off without DCS

A: Indeed, we should dedicate one meeting on this

Q: How many RU's will there be A: Unknown, since this depends on the RN and the multiplexing. Assume ad interim 100.

Q: The use the existing IEEE960 crates could save a lot of money, shouldn't LHCb make a claim on these crates ? A: Definitely, but also do not forget those crates may need to be checked/ revised

Q: If we avoid using buses in other areas as well and use crates just for power, cooling and housing, the savings could even be higher...

A: Definitely. A VME 9 U crate costs between 15-20 kFS plus rack and cooling (which is undefined) .....For IEEE960 it all exists