

LHCb 2003-005

DAQ

21 January 2003

Using the SPECS in LHCb

Dominique Breton, Daniel Charlet

Laboratoire de l'Accélérateur Linéaire - Orsay

ABSTRACT

This document attempts to describe how to use the SPECS in LHCb. The technical specifications of the bus itself are given in another document [1]. This note presents how the SPECS can be interfaced with the various sub-systems.

Contact : charlet@lal.in2p3.fr, breton@lal.in2p3.fr

1 Context

The SPECS has been designed to allow control of the front-end electronics of LHCb. The system mostly consists of three elements : a bus master located on a PCI board in the counting rooms (see fig 1), a slave in the cavern, delivering JTAG, I2C and a parallel interface to control the electronics, and dedicated software to drive the system from the PVSS II SCADA environment upon which the LHCb ECS system is built.

The board housing the masters is shown on fig 1. It's a PCI board providing 4 RJ45 outputs. Two of them are mixed, which allows the users to drive JTAG or I2C directly from their PC for test bench purpose (for instance). As a slave is integrated within the board, the system behaves like the expanded one. In particular, the software is identical. On the first prototype of the board, the mixed outputs won't provide SPECS.

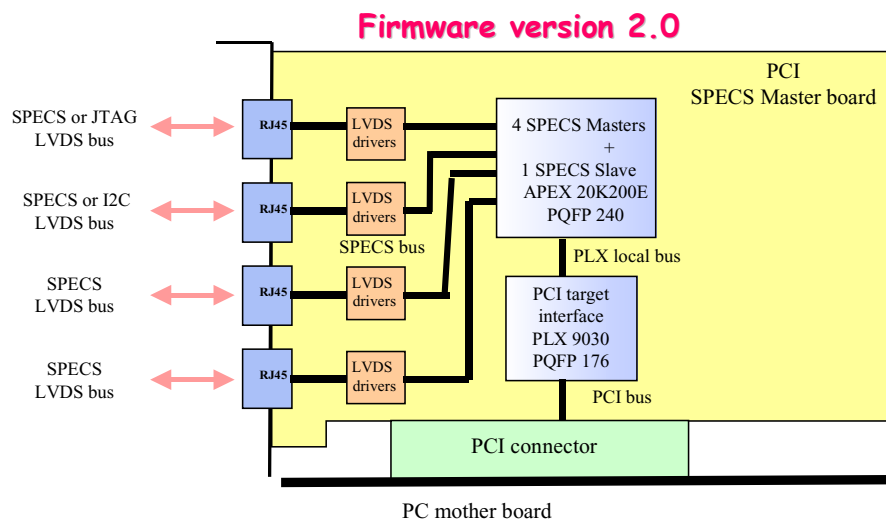


Fig 1 : the SPECS PCI master board.

The technicalities of the protocol between master and slave(s) are described in ref[1] and are not too relevant here. The main discussion concerns indeed the location of the slave, and the types of bus it can deliver.

The slave will be designed as a portable Verilog code and physically integrated in an ACTEL anti-fuse PGA. With this technology, the slave is SEU immune, provided the internal registers are appropriately protected by triple voting techniques, and states machines use one-hot state. It is also reasonably radiation tolerant, up to 10 krads (with some safety factor, the ACTEL chip having been tested up to 40 krads) over the lifetime of the experiment. It can then be placed at most locations where we foresee to have electronics, but not in or near the Velo tank. Fig 2 shows the block diagram of the slave's interconnections. It may also be envisaged by users to use the slave Verilog code as a block within a bigger Actel FPGA.

As shown on fig 2, the SPECS bus is bi-directional, two electrical pairs being dedicated to each direction. On the top side, one can find the different control signals necessary for a proper functioning. On the right side, the parallel I/Os are represented. Finally, the bottom side describes the JTAG and I2C I/Os. It's also envisaged to allow the user to ask for a replacement of the parallel bus if unused by other JTAG or I2C outputs, or maybe even to customize all the outputs depending on the requirements from the host board.

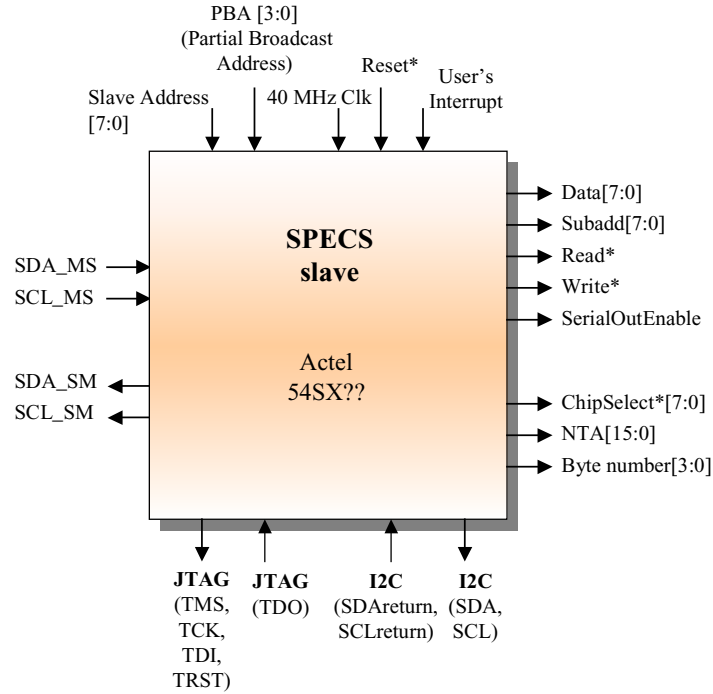


Fig 2 : the SPECS slave.

2 Direct implementation of the slave.

The simplest way to use the SPECS is to place the slave FPGA on the board one wants to control. This gives direct access to JTAG and I2C, together with the parallel bus. One needs to provide the 40 MHz clock (from TTCrx) and to specify the personal and the group broadcast addresses of the slave by jumpers for instance. A RJ45 connector is defined as standard to receive the signal from the master and send it back thereto (see fig 3).

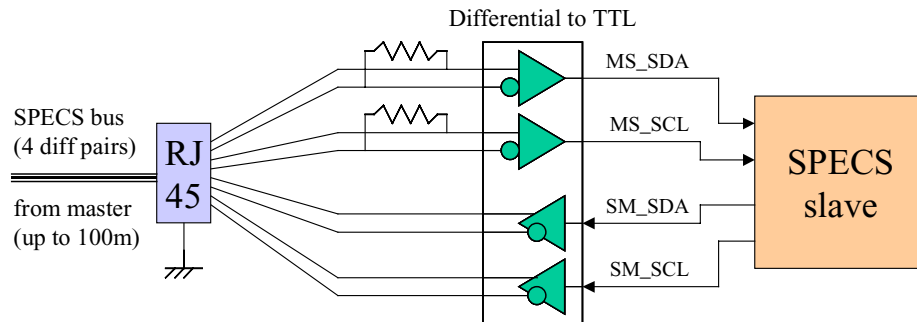


Fig 3 : SPECS slave standard interconnection.

As the same master can drive several slaves (up to 240 different addresses), the SPECS bus may be daisy-chained locally. Be careful anyway not to drive too many slaves with the same physical bus to avoid loading the lines too heavily for obvious signal integrity reasons (32 sounds like a reasonable limit). Impedance adaptation should also be provided at the extremities of the bus. If the master is located far from the slaves' zone, a repeater has to be implemented in the latter (see fig 4). This may imply the use of removable arrays of resistors, to be put on the board for the termination adaptation.

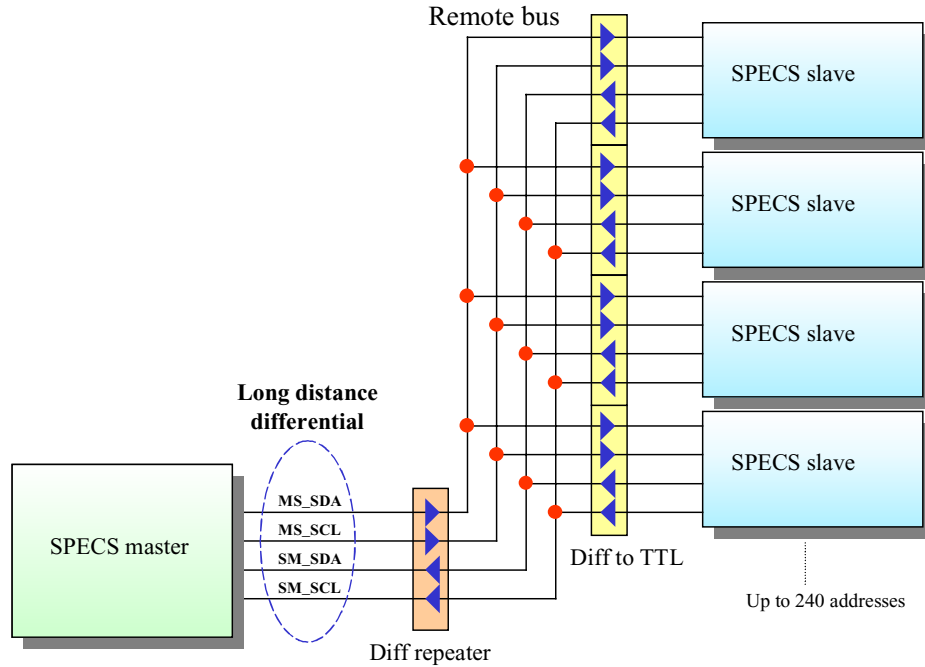


Fig 4 : SPECS remote bus implementation.

The advantage of this method is simplicity. This is the solution we intend to use in the calorimeter. The SPECS bus will actually be distributed on the backplane by the so-called Crate Controller board, which also distributes the TTC signals to all the boards in the crate. This allows us to ensure a perfect integrity to the signals. This dedicated backplane already exists, and is available for use by other detectors. (See ref[2])

3 Implementation using only JTAG or I2C.

In this solution, an intermediate board (6U VME), provided by LAL-Orsay, contains the SPECS slaves, and provides JTAG and I2C connections on its front panel (see Fig 5). The user board needs a RJ45 connector for either JTAG or I2C input, with the proper cabling as described on fig 6. The SPECS system is seen in this case as a JTAG or I2C provider, and its internals can be completely ignored. This option is mandatory for boards situated in high radiation areas, like the Velo on detector boards, for it isn't possible to put the SPECS FPGA at these locations.

Please notice that on fig 6, both remote SDA and SCL have to be sent back to the SPECS slave board to allow a proper sampling, which actually does not depend on the length of the I2C cable.

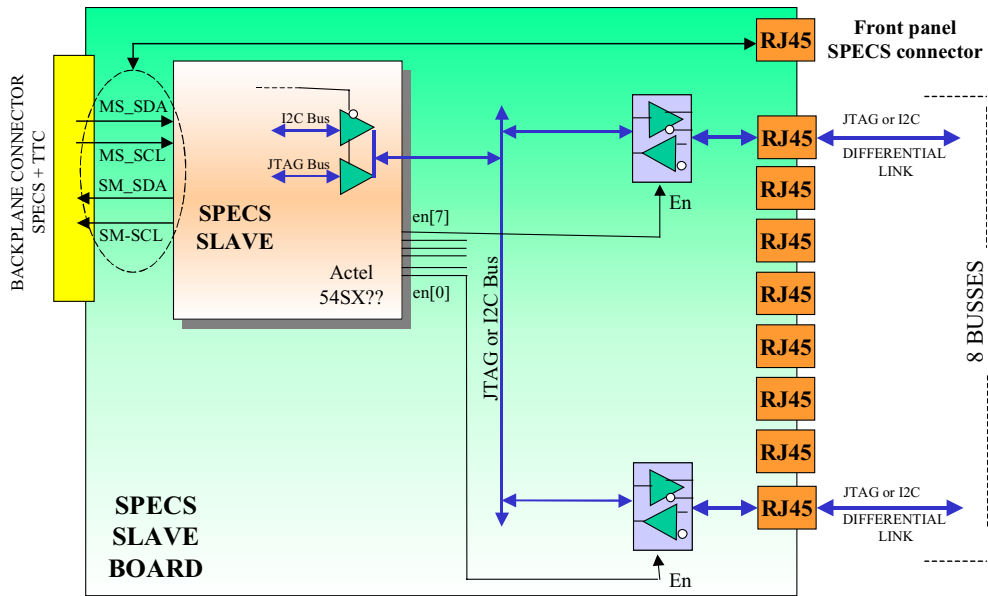


Fig 5 : SPECS slave board.

There are two ways to deliver the SPECS bus to the boards : either using the SPECS lines of the standard calorimeter backplane (see ref [2]) if the required overall crate data bandwidth does not exceed 1MByte/s, or using a dedicated RJ45 connector on the board’s front panel otherwise. These configurations (more detailed in ref[1]) will be selectable thanks to straps located on the board.

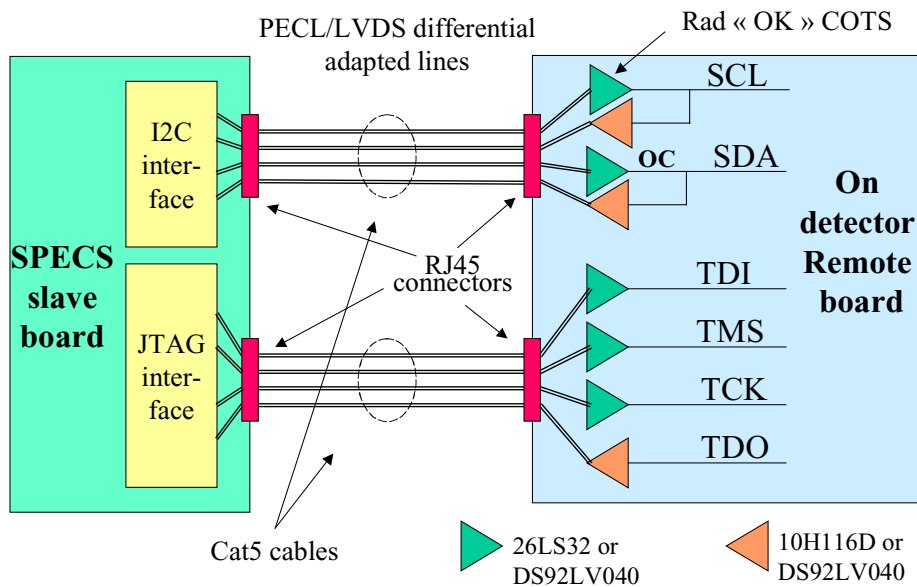


Fig 6 : SPECS slave to detector electronics cabling.

4 Different sub-detector implementations.

The implementations of the SPECS system vary depending on the sub-detector. Possible solutions based on our current understanding of the subsystems are shown below. It’s anyhow very likely that some evolutions already occurred, which may make them obsolete. Please react thereto rapidly, to allow us to update this documentation !

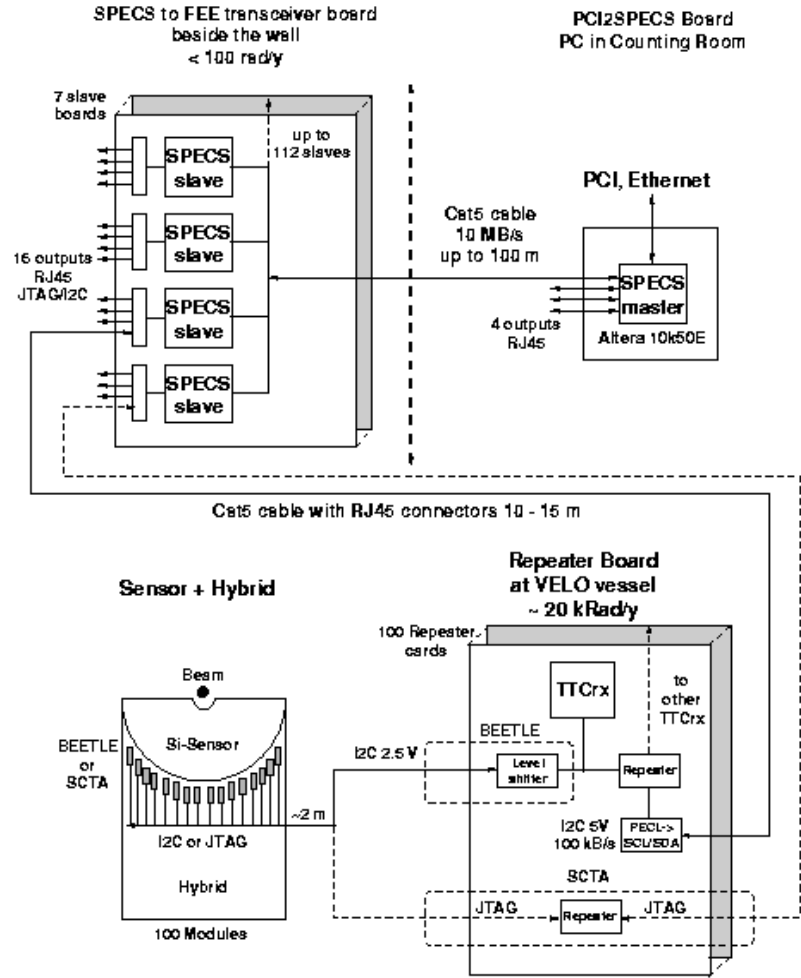


Fig 7 : VELO/Inner Tracker possible implementation.

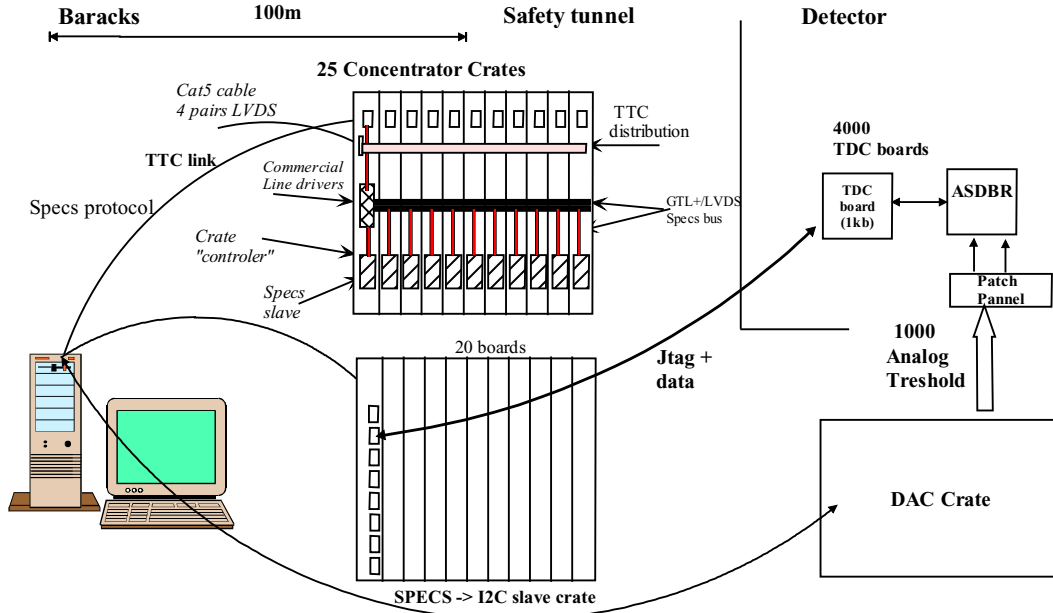


Fig 8 : Outer Tracker possible implementation.

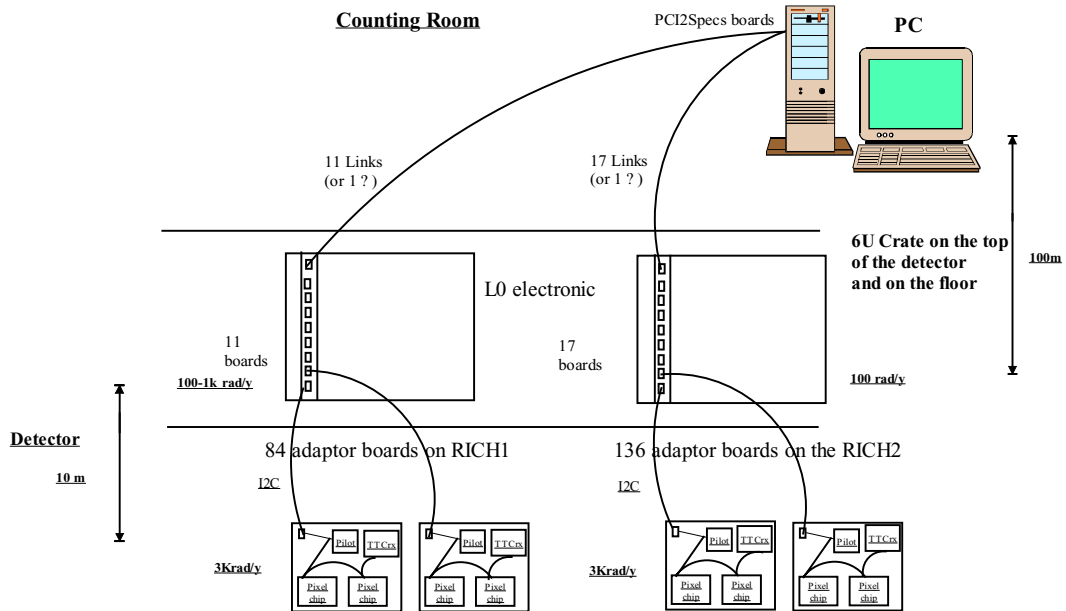


Fig 9 : Rich possible implementation.

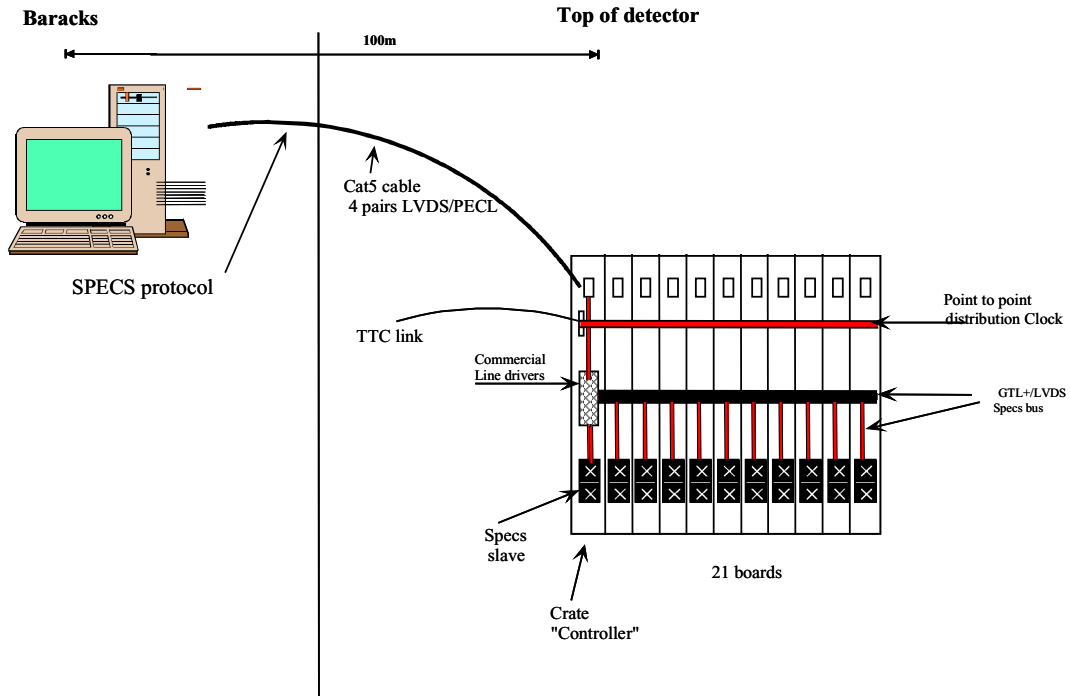


Fig 10 : Calorimeter implementation.

5 References

[1] Serial Protocol for the Experiment Control System of LHCb, Version 2.0, D.Breton and D.Charlet, LHCb note 2003-004.

[2] Powerpoint presentation of D.Charlet about the common calorimeter backplane at the calorimeter electronics review, July 2002,
<http://doc.cern.ch/AGE/current/askArchive.php?a02959/a02959s1t3/transparencies/Charlet.pdf>.