Timing and Fast Control

LHCb Technical Note

Issue: 2
Revision: 2.0

Reference: LHCb DAQ 2001-16
Created: 1st June 1998
Last modified: 15 June 2000

Prepared By: Richard Jacobsson / CERN
B. Jost / CERN

LHCb DAQ Group

Abstract

In this paper we discuss the current understanding of the design of the LHCb Timing and Fast Control (TFC) system. In view of the fact that there exists some infrastructure for a TFC in the form of the RD-12 TTC system we focus on the applicability of this system to the LHCb TFC, subject to the special LHCb requirements imposed by the LHCb two-level trigger architecture. We conclude that the RD-12 system can be used for our application, but that we have to build a few modules to support our high Level-0 accept rate (Readout Supervisor) and to support the requirement of partitioning (Switch). We expect no major problems in implementing both modules.

Document Status Sheet

Table 1 Document Status Sheet

1. Document Title: Timing and Fast Control			
2. Document Reference Number: [Document Reference Number]			
3. Issue	**4. Revision**	**5. Date**	**6. Reason for change**
Draft	0.5	1 Jun 97	First Draft
1	1.0	26 January 1999	First release
2	2.0	26 May 2000	Update TFC Architecture

Table of Contents

List of Figures

List of Tables

1 Introduction

LHCb requires a Timing and Fast Control (TFC)[1] system to distribute information that must arrive synchronously at various places in the experiment. Examples of this kind of information are

- Beam-synchronous clock
- Trigger decisions (Level-0 and Level-1)
- Reset and synchronisation commands
- Bunch Crossing number and event number

The TFC system also needs to provide facilities to compensate for

- Particle Time-of-Flight
- Detector & electronics delays
- Propagation delays in cables

Since the beginning of the LHC experimental program it was recognised that the TFC system is an item of common interest to all experiments and should therefore be a common R&D project. As a consequence the RD12 collaboration was set-up and subsequently developed a TFC system (RD12-TTC see Ref. [1]). Given that the RD-12 TTC system is existing we have extensively studied the question how it can be applied in LHCb.

Since LHCb uses the same or similar detection techniques as ATLAS and CMS we assume that the 'performance" specifications of the RD12 system, which are a result of the requirements of ATLAS and CMS, are also satisfactory for LHCb[2].

The document is structured as follows. In Chapter 2 we will discuss the general and LHCb specific requirements on a TFC system. In Chapter 3 the general architecture of the TFC system in LHCb will be described. In Chapter 4 we shortly discuss the way we intend to operate the system.

This note is intended to give an overview of the conception of the LHCb TFC system. It is not intended to describe the components and operational procedures in detail. These will be described in separate notes.

This Document is an update of a previous LHCb technical note (LHCb DAQ 99-001). The update was necessary mainly because the architecture of the TFC system has changed somewhat to support multiple concurrent multi-detector partitions. In addition a scheme for a fast throttling mechanism was added to the system that would allow to throttle either the Level-0 or Level-1 trigger within less than a micro-second, which in turn allows to simplify the algorithms that decide when to apply the throttle significantly. The main changes have been in sections

3.2.1 (Readout Supervisor) where basically the block diagram has been updated.

3.2.3 (TFC Switch) The switch is a new component replacing the 2:1 switches of the original architecture

3.2.4 (Throttle Switches) The Throttle-Switches are new components which support the fast trigger throttling

[1] We deliberately use the acronym TFC to distinguish it from the RD-12 TTC, since the TTC is only part of a bigger system.

[2] This needs to be verified once detailed designs, especially of the Front-end electronics, of the different sub-detectors of LHCb are available.

2 Requirements on a Timing and Fast Control System

2.1 General Requirements

The basic task of the TFC system is the synchronous transmission of information from a central point to all components of the LHCb detector where this information is needed e.g. Level-0 electronics and Level-1 electronics. This requirement implies a high-multiplicity fanout network (typically 1:1000).
As mentioned in chapter 1 we do not expect the LHCb 'performance' requirements like clock frequency or clock jitter to be significantly different from those of ATLAS or CMS. All LHCb detectors will have shaping times of their analogue signals of the order of 25 ns or more and for example the RICH detector has intrinsic path differences in the HPDs of 0.5 ns. We therefore conclude that even though the exact requirements are not yet known the contents of the following table are justified.

Parameter	LHCb Requirement	RD12 TTC Specifications
Clock Frequency	Beam Synchronous (~40 MHz)	Beam Synchronous (~40 MHz)
Number of Clock phases	≥2	2
Range of phase adjustments	Few 100 ns	400 ns
Resolution of phase adjustments	Few 100 ps	~100 ps
Clock jitter	<200 ps	35 ps-129 ps (RMS)[3]
Level-0 Trigger transmission rate	40 MHz	40 MHz
Level-1 Trigger transmission rate	~1 MHz	Not foreseen (see below)

Table 2 Summary specifications of the LHCb Requirements and the RD12 TTC specifications

2.2 LHCb Specific Requirements

The Level-0 trigger decisions (like the Level-1 trigger in ATLAS and CMS) obviously have to be transmitted at the rate of the LHC clock, i.e. 40 MHz. LHCb has one special basic requirement on the TFC, namely the necessity to transmit a second level of trigger decisions to the front-end electronics (Level-0 Electronics and Level-1 Electronics). The rate of these decisions is equal to the rate of Level-0 accepts and is estimated to be 1 MHz. There is no direct provision in the RD12 TTC system for this functionality, however there seems to be a mode of operation of the RD-12 system, which would allow us to implement it (see section 3.1)

2.3 Partitioning

From past experiences in the LEP experiments the feature of partitioning the readout system is considered to be very important. By Partitioning we mean the possibility to sub-divide the LHCb DAQ system into different disjoint independent sub-systems. Each of these sub-systems will have its own trigger source and its own part of the readout electronics. This implies that the TFC will also have to be able to be partitioned, i.e. different parts of the detector will have to receive different trigger signals[4]. This has consequences for the possible architectures of the TFC. We are putting effort into studying the implications of partitioning in all areas of the system.

[3] The jitter on the clock depends on the activity of Channel B of the TTC system. This activity is quite high in LHCb, since there will be Level-1 trigger decisions transmitted over Channel B at a rate of 1 MHz.

[4] For the time being we assume that all partitions use the same clock

3 General Timing and Fast Control Architecture

Figure 1 shows the general architecture of the timing and fast control system as envisaged for the LHCb experiment using the RD12 TTC system.

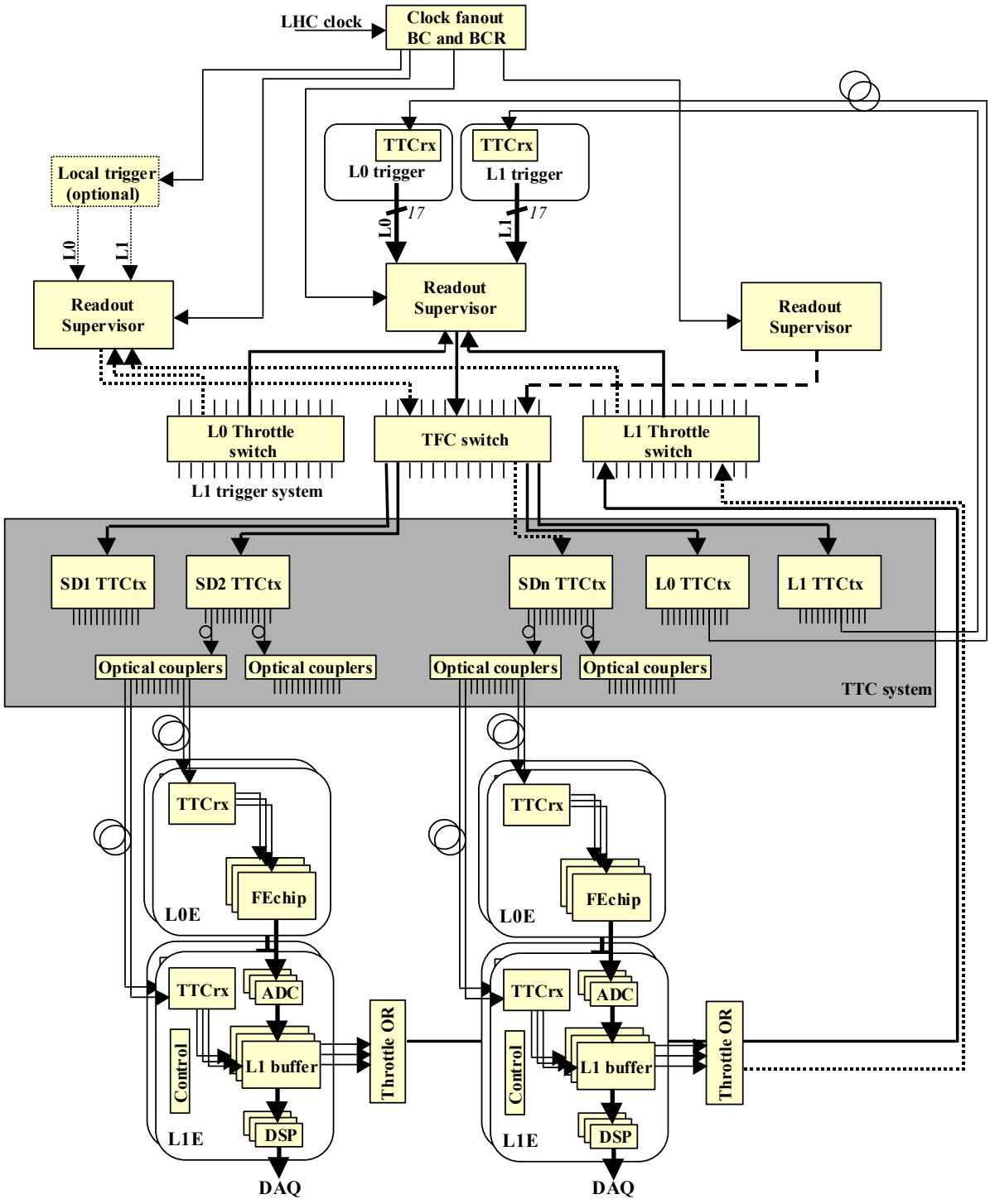

Figure 1: General Architecture of the Timing and Fast Control system

3.1 Operation of the RD-12 TTC System

The RD-12 TTC system is operated in the following way:
Channel A is used as it was intended, to transmit the beam-synchronous clock and the LHCb Level-0 decision to the Front-end electronics.
Channel B of the system was intended to transmit configuration commands to individual receiver chips. This functionality is not needed anymore since the new version of the receiver chip has now a I^2C interface integrated that will allow to set them up through the Experiment Controls System (ECS). Hence Channel B becomes free for other use and we intend to use it to convey the LHCb Level-1 trigger decision to the receiver chips. Obviously the Level-1 decision has to arrive synchronously at all receivers. For this reason we intend to use the broadcast feature of Channel B which allows sending synchronously information to all receivers. According to the RD-12 specifications the bandwidth of Channel B is 40 Mb/s and the length of a short broadcast frame is 16 bits out of which 6 bits can be user defined. Hence a repetition rate of 2.5 MHz of broadcasts seems to be possible. This number has to be verified in a test. Another possibility would be to use a mode of operation of channel B called the long broadcasts that would allow transmitting up to 16 bits of user defined information. The frame length in this case is 42 bits which would allow a repetition rate of ~950 kHz. This latter figure seems to be very marginal compared to the expected Level-1 decision rate of 1 MHz in average. Channel B will also be used for other synchronous commands like e.g. reset commands to the Level-0 and Level-1 electronics and commands to inject test pulses in the detector electronics.

3.2 Description of the Components of the System

In the following sections we give a short functional description of the key elements of the system depicted in Figure 1.

3.2.1 Clock Distribution

We foresee the distribution of a common clock originating from a single point to the entire experiment. The distribution will be done through a fanout and subsequently through the TTC system (TTCtx) to the equipment. This scheme guarantees synchronism throughout the experiment. The RD-12 collaboration has designed a module that will receive the clock and the bunch-counter-reset signal from the LHC control room and provide the necessary fanout functionality (TTCmi).

3.2.2 Readout Supervisor

The Readout Supervisor (RS) is the central point of the TFC system. It receives the clock and the trigger decisions and transmits this information via the TTC transmitter (TTCtx) to all equipment that needs it. It will also receive commands from the control system, for example to enable/disable the trigger[5]. A block diagram of the RS showing the main functional components is depicted in Figure 2.
It should be noted that disabling the trigger does not have any effect on the trigger machinery itself. The trigger hardware will always decide based on the data that arrive from the detector. However the RS will gate the signals of the trigger system according to the state of the readout system.
The RS will keep an overview of the state of buffers in the Level-0 electronics that run synchronously to the clock and hold off Level-0 triggers should there be a danger that those buffers overflow. It will also receive hardware throttle signals originating from other parts of the readout system, like e.g. the L1 Electronics boards or the Level-1 trigger system. The Trigger throttling as described in Ref. [2] will be implemented in the RS using the same mechanism as for disabling the trigger. The RS will implement other rules governing the dataflow like, emptying the Level-0 derandomizer buffer before resetting the Level-0 electronics.
The RS will keep counters that allow monitoring its performance and the performance of the experiment (dead-time) using the ECS interface. The RS will also provide data to the DAQ on an event-by-event basis since it is the only place where the "true" bunch crossing ID and Event Number are known.
Another feature of the RS will be the autonomous generation of triggers, either on a periodic basis, or distributed

[5] Actually enabling/disabling the trigger really means enabling/disabling the readout of data.

randomly according to Poisson distributions with programmable rates.

The encoding of the signals for the TTC system will be done in the RS, since the current implementation of the TTCtx expects the signals already encoded.
An LHCb note concerning the detailed RS specifications is in preparation.

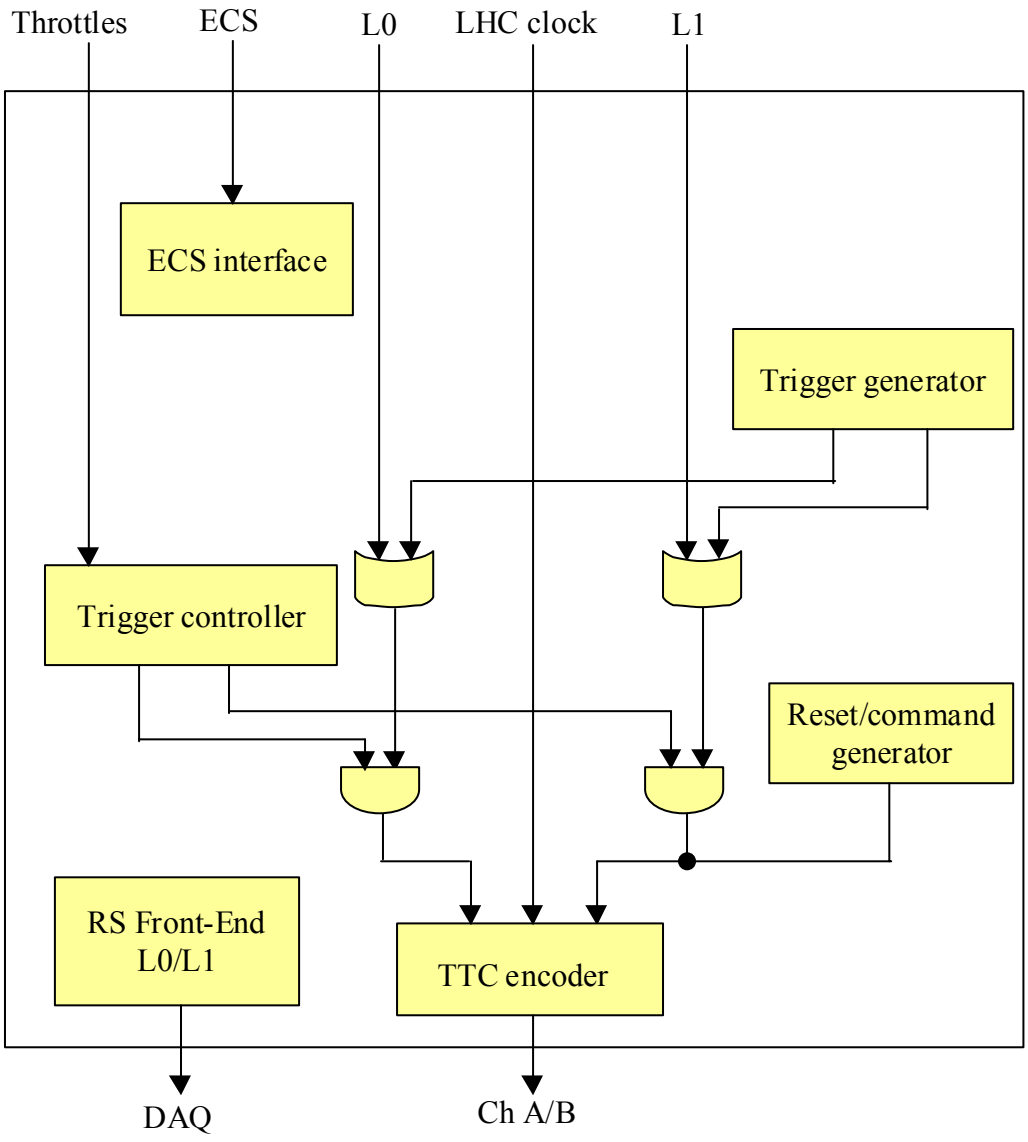

Figure 2 Block diagram of the Readout Supervisor

3.2.3 TFC Switch

The switch module allows choosing from which RS the TTCtx' should receive timing, trigger and control signals. The switch allows associating any set of output channels to one input channel, which would in the given configuration drive the TTCtx' connected to the output port. Thus the sub-systems connected to these TTCtx' can be run coherently and independent of other sets of TTCtx' that are connected to another RS. Any number of combinations of disjoint sets of output ports is possible. Initial specifications are 16 input and 16 output ports.

3.2.4 Throttle Switches

The function of the throttle switches is to feed back the throttle information to the appropriate RS, such that only the RS that is driving a data stream is throttled by electronics within that data stream. The logical operation of the throttle switch is to do a logical OR of the inputs associated to the data stream. Usually the set of inputs is the same as the set of outputs of the TFC switch there can however be cases where a sub-system wants to receive the trigger decisions and timing information, without throttling the trigger (SPY mode). There are two throttle switches, one to throttle Level-0 triggers and one to throttle Level-1 triggers. Typically The Level-1 trigger is throttled by the readout system and the Level-0 trigger by the components that feed the Level-1 trigger system.

A detailed functional specification document concerning the TFC and the Throttle switch is in preparation.

3.2.5 TTCtx

The Function of the TTCtx is to receive the encoded information for the channels A and B of the TTC system and transmit it through the passive optical fanout network [1].

3.2.6 TTC Optical Fanout

This is a passive optical system using splitters to further distribute the input to the outputs. Since it is passive, it cannot be configured and can only be used in one direction, i.e. No information, like a "Busy" signal, can be sent back from the far side towards the TTCtx.

3.2.7 TTCrx Chip

The TTCrx is the receiver chip of the signals originating from the TTCtx. It is implemented in a rad-hard technology so it can be used also in a high radiation environment. For completeness we summarise the main functionality of the TTCrx chip here (see Ref. [1] for details). The TTCrx chip reconstructs the LHC clock from the encoded signals originating from the TTCtx. It supplies in addition two additional clocks synchronous to the original clock with adjustable phases. These two signals can be used by the Level-0 Electronics to clock the analogue signals into the L0 Pipelines and clock the data out of the pipeline upon a L0 Yes decision. The phases of these operations do not necessarily have to be the same.
The TTCrx chip also decodes the Channel B information and provides it on the output pins of the chips. Further interpretation of this information has to be done externally to the chip on the Front-End boards or Hybrids.
The chip can be configured to provide a bunch-crossing counter (bunch relative to the LHC cycle) to which the L0 Yes decision applies and an event counter which is incremented for each Level-0 Yes decision. The latter feature of the chip can however not be used in LHCb because of the high Level-0 trigger rate of 1 MHz. The use of the event counter would imply to be unable to accept Level-0 triggers in two successive clock cycles. Hence the event counter has to be implemented in a counter external to the TTCrx chip which is possible because the necessary signals are available.

3.2.8 Level-0 Electronics (L0E)

The Level-0 Electronics (L0E) holds all electronics necessary to capture the signals from the detector and store them for the duration of the Level-0 trigger. See e.g. Ref. [3] for details on the architectures of the front-end chips. After a positive Level-0 decision has been issued the data are logically transferred into a de-randomising buffer for subsequent readout. During the readout the data are multiplexed 32:1 onto links to the Level-1 Electronics (L1E). The L0E will provide in addition to the detector data information that allows detecting de-synchronisation within a set of front-end chips. Mechanisms for this are described in Ref. [4].
For sub-detectors whose data are used in making the Level-0 trigger decision there will be a second data path off the L0E for this purpose.

3.2.9 Level-1 Electronics (L1E)

The L1E holds all necessary electronics to buffer the data for the duration of the Level-1 trigger processing and to zero-suppress the data before they are fed into the DAQ system. It is foreseen that at least some sub-detectors will use DSPs to perform the zero-suppression. The possibility to have a common module within LHCb where the detector specific parts would be encapsulated in the input stage of the L1E and in the code running on the DSP, is still under investigation. The L1E will implement the necessary hardware to provide the data for checking synchronisation as mentioned in section 3.2.8. In particular it will implement an emulator, or the equivalent thereof, of the L0E buffers to allow a synchronous readout scheme, i.e. to rely only on the common clock of the system for reading out the L0E.

3.3 Consequences of the Architecture

The architecture outlined above has some implications on the operation of the system. In the following sections we describe the most important issues

3.3.1 Partitioning

The architecture outlined above supports partitioning. It is important however to be aware of the finest granularity, i.e. the smallest component of the system that can be read out and triggered independently of the other components of the system. Since the optical fan-out network is passive, and hence not programmable, the finest partitioning granularity at this level is the TTCtx. Assuming that each sub-detector will have its own TTCtx, the finest granularity will thus be one sub-detector. For example, it will not be possible to read out all but one chamber of the Inner Tracker within the LHCb partition (the whole experiment) and debug the one chamber that is left out in stand-alone mode.
Suppression of the read-out of faulty parts of the detector has to be done in the Level-1 electronics, since it is, in the current version of the TTCrx chip[6], not possible to ignore the Level-0 decision in the TTCrx chip. Hence the FE chips will always send their data to the Level-1 electronics.
A detailed note on all aspects of partitioning also beyond the TFC sub-system is in preparation.

3.3.2 Error Reporting and Handling

As is mentioned earlier, the TTC system is uni-directional, i.e. information is only flowing from the TTCtx towards the TTCrx. The mechanism foreseen to implement a reverse path is the general experiment control system. This system however is not designed to be fast, definitely not at the level of the LHC clock period. Hence a lot of effort has to be put into the problem of error detection, since from the moment of detecting an error and until appropriate corrective action is taken, significant time periods can elapse. During this time period many events will reach the L0E and L1E.
For some types of errors all these events will have to be flagged as erroneous, until a reset operation is performed. One could envisage the implementation of a reverse information path from the L0E or the L1E to the RS, however given the propagation delays there is no way to disable the trigger before the next clock cycle. Hence this would not really solve the issue, just perhaps reduce its scale. Of course this depends very strongly on the rate at which errors will occur in the system and what the impact of these will be on the physics data. A periodic reset scheme could be envisaged, such that every turn or every ***n*** turns of the machine where there is a period of ~3.0^7 μs without particles all the L0E buffers (pipelines and de-randomizers) could be reset, independently of whether an error has occurred or not. The strategy for resetting parts of the system is currently under study[5].
It is very important that provisions are made in the system to detect errors by providing information that can be checked at higher levels in the readout of the data against locally generated information. This problem is discussed in Ref. [4]

[6] Only the interpretation of the Channel-B commands is possible in the current version of the TTCrx chip.

[7] Actually there are de-facto two such gaps per turn of the machine in LHCb due to the bunch structure of the LHC accelerator and the location of LHCb on the ring.

3.3.3 Estimated Scale of the System

Table 3 gives estimates on the number of components of each type needed to implement the LHCb TFC system. Certain assumptions have been made, such as:
Each sub-detector will have its own TTCtx
Each sub-detector will have a local trigger
One TTCrx will feed 10 FE chips which in turn will handle 128 channels each
One TTCrx on the L1E corresponds to one TTCrx on the L0E[8]
There is not yet a detailed analysis done concerning the exact distribution of TTCrx' to FE Chips etc.

Item	Number	
Clock Fanout	1	(Part of TTCmi, TTC Machine Interface)
RS	<16	
TFC Switch	1	
Throttle Switch	2	One for L0 and one for L1
TTCtx	<16	At least one per Subdetector
TTC Optical Splitter	<16	At least one per Subdetector
TTCrx	~2000	50% L0E, 50% L1E

Table 3 Estimated Number of different components needed to implement the LHCb TFC system

[8] Alternative schemes to reduce the number of TTCrx chips are being studied, like e.g. to use only one TTXrx chip per L1E board and use multi-channel delay chips to adjust the timing for the different links from the L0 electronics. This scheme could reduce the number of TTXrx chips for the L1E from 1000 to ~300.

4 Operation

The operation of the TFC system can be divided into several activities or phases

- Power-up sequence
- Timing Calibration
- Initialisation sequences
- Data-taking

4.1 Power-Up Sequence

Once the TTC system is powered the clock is distributed to the whole experiment. As soon as the clock is being delivered, data gets clocked into the L0 pipeline and gets transmitted to the L0 trigger. However the RS will always send out Level-0 "No" decisions irrespective of the Level-0 trigger decisions until the all components of the system are initialised and the trigger enabled. It is not foreseen to deliberately stop the clock distribution.

4.2 Timing Calibration

During timing calibrations the values of the phase shifts for every TTCrx chip are determined. These values are loaded into the TTCrx chips during initialisation. The mechanism for the determination of the delays is subject to a separate study.

4.3 Initialisation

During the initialisation phase of the system the internal parameters of the RS, the L0E and the L1E will be loaded using the control system. This operation includes setting-up of the phase delays obtained from the timing calibration in the TTCrx chip. At a certain stage of the initialisation sequence, the RS will send out a reset command (using a Channel B broadcast) that will synchronise all the L0E and L1E, e.g. resets the write pointers of the pipelines to the start and flush the de-randomising buffers. From this moment on the L0E and L1E are ready to receive triggers.

4.4 Data-Taking

This mode is entered after the initialisation has completed. The RS will eventually be enabled to transmit positive trigger decisions. When a positive Level-0 decision is transmitted to the L0E the readout of the data into the L1E is initiated and data will be buffered there to await the Level-1 decision. At the same time data are also transferred to the Level-1 trigger electronics. After processing these data a Level-1 decision (reject or accept) is distributed to the TTCrx' located on the L1E[9], which either discard the data or transfer them on for further processing respectively. There will be a Level-1 decision for every event accepted by the Level-0 trigger.
As mentioned in section 3.3.2 the problem of synchronisation loss and re-synchronisation has to be studied. Re-synchronisation can always be achieved by resetting the pipeline pointers and the de-randomising buffers. This is however coupled with potential data losses. Therefore the frequency of resets that will be required has to be understood but can only be done once the scale of the de-synchronisation problem is known[10]. The RS must have a provision to set

[9] Actually the Level-1 decision is also received by the TTCrx chips on the L0E, but is subsequently ignored there

[10] This scale might only be known some time after the LHC startup, since it can well be that the irradiation of the equipment has a significant impact on the rate of de-synchronizations.

up this frequency and it must also be possible to initiate a reset sequence through the control system ("reset on demand").

5 Conclusion

We have discussed the applicability of the RD-12 TTC system to the problem of the LHCb Timing and Fast Control. We have devised and architecture and a mode of operation such that we believe that the TTC system can satisfy the LHCb requirements, in particular the distribution of a second trigger decision, which was not foreseen in the design of the TTC system. This must be confirmed in the lab by making real tests.
A few modules will have to be designed specifically for LHCb (RS, Switches), but we foresee no major problem.
Points to be studied are the error rates on the TTC system (in particular after the TTCrx chips have been irradiated) and the maximum rate of broadcasts that can be sent out through the TTC system

6 Glossary of Terms

Front-End Electronics	Summary term for the Level-0 Electronics and the Level-1 Electronics
L0E	Level-0 Electronics. It holds the buffers (pipelines) to bridge the latency of the Level-0 trigger and a de-randomising buffer to cope with the random arrival of Level-0 triggers. It also contains all electronics needed to transfer the data to the L1E.
L1E	Level-1 Electronics. It hold the buffers for the data to bridge the latency of the Level-1 trigger and processing elements to perform Zero-Suppression.
TFC	Timing and Fast Control system of LHCb. It uses the TTC system but has a wider scope.
TTC	Trigger Timing and Control system developed in the framework of the RD-12 collaboration
TTCrx	TTC Receiver. A chip that receives the information from the TTCtx and recovers a synchronous clock and the Level-0 decisions. It also makes the contents of the Channel B broadcasts available.
TTCtx	TTC Transmitter. Unit to transmit the encoded TTC information through the optical distribution network
ECS	Experiment Controls System.

7 References

[1] RD-12 Documentation on WWW (http://www.cern.ch/TTC/intro.html) and references therein

[2] M. Frank et al "DAQ architecture and read-out protocols" LHCb Technical Note, LHCb 98-028 (unpublished)

[3] LHCb Collaboration, LHCb Technical Proposal, LHCC-98-04

[4] Y. Ermoline et al., "Vertex Detector Electronics - Timing and Synchronization Issues", LHCb Technical Note, LHCb-98-052 (unpublished).

[5] See the presentations of J. Christiansen and H. Dijkstra at the LHCb front-End Electronics/DAQ/Controls workshop held May 2000.