- Readout Supervisor -

Outline

- Readout Supervisor role and design philosophy
- Trigger distribution
- Throttling and buffer control
- BCRs & Resets
- Auto-triggering for calibration & test
- Priority scheme between L1/resets/commands
- Errors detected by RS
- Counters
- RS data block
- Discussion topics

Note: No recipes just flexible machinery! Feedback!
Design philosophy

- Flexible and versatile
- Simple
- No internal intelligence --> configured by ECS
- Accounting
- Transparent --> debugging
- Reliable
Specifications

RS Design Specification document underway:

Table of Contents

1 INTRODUCTION .................................................................................................................................

2 FUNCTIONAL SPECIFICATIONS ........................................................................................................
  2.1 INTRODUCTION .................................................................................................................................
  2.2 READOUT SUPERVISOR SYNCHRONISATION ......................................................................................
  2.3 LEVEL-0 trigger distribution ...............................................................................................................  
  2.4 LEVEL-1 trigger distribution ...............................................................................................................  
  2.5 READOUT SUPERVISOR DATA ..........................................................................................................  
  2.6 FRONT-END/DAQ BUFFER OCCUPANCY CONTROL AND THROTTLING ...........................................
  2.7 BUNCH COUNTER RESET (BCR) .........................................................................................................
  2.8 FRONT-END RESET GENERATION ....................................................................................................
  2.9 ONLINE DETECTOR CALIBRATION/MEASUREMENTS ........................................................................
  2.10 STAND-ALONE DETECTOR CALIBRATION/MEASUREMENT RUN ...................................................
  2.11 TEST/DEBUG RUN ............................................................................................................................
  2.12 OTHER COMMANDS TO THE FRONT-END .....................................................................................
  2.13 COUNTERS ....................................................................................................................................
  2.14 THE ECS INTERFACE ......................................................................................................................

3 MODULAR SPECIFICATIONS ...............................................................................................................
  3.1 INTRODUCTION .................................................................................................................................
  3.2 RS BOARD STANDARD .......................................................................................................................  
  3.3 THE ECS INTERFACE .........................................................................................................................
  3.4 COUNTERS .......................................................................................................................................
  3.5 ADJUSTABLE DELAYS .......................................................................................................................  
  3.6 RANDOM GENERATOR .........................................................................................................................
  3.7 LEVEL-0 trigger distribution ...............................................................................................................  
  3.8 LEVEL-1 trigger derandomizer ...........................................................................................................
  3.9 TRIGGER, RESET AND CONTROL COMMAND SEQUENCER ......................................................
  3.10 TTC ENCODER .................................................................................................................................
  3.11 TTC ENCODER .................................................................................................................................
  3.12 FRONT-END BUFFER EMULATION ....................................................................................................
  3.13 RS DATA PIPELINE/BUFFER .............................................................................................................
  3.14 EXTERNAL TRIGGER .........................................................................................................................
  3.15 INTERNAL OSCILLATOR ......................................................................................................................
  3.16 CLOCK INHIBIT .................................................................................................................................

4 SUMMARY I/O INTERFACES, STATUS LEDS ...................................................................................

5 GLOSSARY OF TERMS .........................................................................................................................

6 REFERENCES ...........................................................................................................................................
RS block diagram

- Forcing triggers
Throttling and buffer control

Overflows:

- L0 de-randomizer emulated --> internal L0 throttle
- L1 trigger system --> hardwired L0 throttle
- L1 derandomizer --> throttle central or cabled
  - central assumes fixed length zero-suppression
  - cabled to RS means FE monitoring + cabling
- Front-End Multiplexing or Readout Units --> hardwired L1 throttle
- Subfarm Controllers --> L1 software L1 throttle via ECS

Counters, timers, time-outs and history buffer for throttles

- On time-outs --> ECS interface raise alarm with throttle type

Count dead-time and losses
Sequencers to implement the various resets:
   - Bunch Counter reset

Programmable timing:
   - Reset L0 pipeline+derandomizer at regular intervals in phase with orbit signal
   - Reset L1 FE at regular intervals in phase with orbit signal
   - Single resets triggered by ECS, transmitted at pre-specified cycle

- BCR highest priority
  - BCR + other resets simultaneously
Calibration & test

- Programmable sequencers
- Forcing auto-triggers
- Available online and stand-alone
- Auto-triggering:
  - Pre-defined intervals -- pedestals etc
  - Consecutive bunch sampling -- timing
  - On calibration pulse -- fired by TTC command
  - Random trigger -- minimum bias
- Stand-alone calibration
  - All of the above
- Stand-alone test with or without local trigger
  - Pre-scalable L0 random trigger (max 1.5 MHz, Poisson)
  - Pre-scalable L1 random trigger (max 200 kHz, Poisson)
Channel B priority scheme

- Priority scheme on channel B:
  1) Resets / Auto-triggers / commands
  2) L1 decisions

- Reset / auto-triggers / commands --> equal priority
  - Sequencer time structure checked before down-load to prevent conflicts (software)
Errors detected by RS

- Errors:
  - L0 strobe missing
  - L0 de-synchronization
  - L1 missing (max latency exceeded?)
  - L1 de-synchronization
  - Buffer overflows
  - Throttle time-outs

- Initially mark & keep erroneous events, later configure automatic rejection/recovery

ECS interface raise alarm
Optional: reject + direct reset
Counters

- LHC bunch clock
- LHC orbit clock
- Bunch ID
- Event ID
- L0 accepts
- L1 accepts
- Missing L0 strobes
- L0 bunch ID error
- L1 event ID error
- L0 derandom. overflows (internal L0 throttle)
- L0 HW throttles
- L1 HW throttles
- L0 SW throttles
- L1 SW throttles
- Bunch crossings lost during L0 throttle
- L0 yes’s converted to no’s during each type of throttle
- L1 yes’s converted to no’s during each type of throttle
- Throttle time-outs

- Resets (different levels)
- Bunch crossings lost during resets
- L0 yes’s converted to no’s during resets
- L1 yes’s converted to no’s during resets
- Forced level-0 accepts
- Forced level-1 accepts
- Self-triggers generated by sequencers

*ECS interface polls over counters and status registers to monitor and alarm
RS data block

- Readout Supervisor “Front-End” handles the RS data block:
  - Bunch ID
  - Event ID
  - Status information provided through front-panel input
  - Event type (physics, random, calibration, empty crossing, test, special)
  - Level-0 and level-1 force bits
  - Error blocklet
## Interfaces

<table>
<thead>
<tr>
<th>Input/output</th>
<th>In/Out</th>
<th>Specification</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>BC in</td>
<td>In</td>
<td>LHC bunch clock from TTCmi</td>
<td>Lemo</td>
</tr>
<tr>
<td>BC out</td>
<td>Out</td>
<td>LHC bunch clock output</td>
<td>Lemo</td>
</tr>
<tr>
<td>BCR in</td>
<td>In</td>
<td>LHC turn signal from TTCmi</td>
<td>Lemo</td>
</tr>
<tr>
<td>BCR out</td>
<td>Out</td>
<td>LHC turn signal output</td>
<td>Lemo</td>
</tr>
<tr>
<td>L0 in</td>
<td>In</td>
<td>L0 trigger decision with 12-bit bunch id + forced L0 bit + strobe</td>
<td>17-pin parallel</td>
</tr>
<tr>
<td>L0 in (aux)</td>
<td>In</td>
<td>Auxiliary L0 trigger from any source</td>
<td>Lemo</td>
</tr>
<tr>
<td>L0 out</td>
<td>Out</td>
<td>L0 trigger decision output for monitoring</td>
<td>Lemo</td>
</tr>
<tr>
<td>L1 in</td>
<td>In</td>
<td>L1 trigger decision with 12-bit event id + forced L1 bit + strobe</td>
<td>17-pin parallel</td>
</tr>
<tr>
<td>L1 out</td>
<td>Out</td>
<td>L1 trigger decision output for monitoring</td>
<td>Lemo</td>
</tr>
<tr>
<td>TTC out</td>
<td>Out</td>
<td>Channel A/B encoded and serialized</td>
<td>1 or 2 Lemo ?</td>
</tr>
<tr>
<td>Throttle L0 in</td>
<td>In</td>
<td>L0 throttle input, eg from L1 trigger system</td>
<td></td>
</tr>
<tr>
<td>Throttle L0 out</td>
<td>Out</td>
<td>L0 throttle output for monitoring</td>
<td></td>
</tr>
<tr>
<td>Throttle L1 in</td>
<td>In</td>
<td>L1 throttle input, eg from L1E</td>
<td></td>
</tr>
<tr>
<td>Throttle L1 out</td>
<td>Out</td>
<td>L1 throttle output for monitoring</td>
<td></td>
</tr>
<tr>
<td>Status in</td>
<td>In</td>
<td>Status information + strobe</td>
<td>130-pin parallel?</td>
</tr>
<tr>
<td>RS data</td>
<td>Out</td>
<td>RS data to DAQ</td>
<td>S-link</td>
</tr>
<tr>
<td>Ethernet</td>
<td>In/out</td>
<td>ECS interface</td>
<td>Ethernet</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>LED</th>
<th>Specification</th>
<th>Colour</th>
</tr>
</thead>
<tbody>
<tr>
<td>On/Off</td>
<td>Power on</td>
<td>Green</td>
</tr>
<tr>
<td>BC ext</td>
<td>External bunch clock present</td>
<td></td>
</tr>
<tr>
<td>BC int</td>
<td>Internal bunch clock used</td>
<td></td>
</tr>
<tr>
<td>BCR ext</td>
<td>External orbit clock present</td>
<td></td>
</tr>
<tr>
<td>BCR int</td>
<td>Internal orbit clock used</td>
<td></td>
</tr>
<tr>
<td>L0</td>
<td>L0 trigger present</td>
<td></td>
</tr>
<tr>
<td>L1</td>
<td>L1 trigger present</td>
<td></td>
</tr>
<tr>
<td>Thrtl L0</td>
<td>L0 throttle asserted, stretched on-time</td>
<td></td>
</tr>
<tr>
<td>Thrtl L1</td>
<td>L1 throttle asserted, stretched on-time</td>
<td></td>
</tr>
</tbody>
</table>
Conclusions

- Specifications well underway
- Need feedback about additional features and requirements
- First functional and modular specifications to be finalized
  - ~2 months
- Simulation
- Design and prototype 12 - 15 months
Discussion topics

- Command broadcast (non-addressed)
- Addressed commands (individual TTCrx)
- L1 derandomizer throttle, central or cabled
  - central assumes fixed length zero-suppression
  - cabled to RS means FE monitor + cabling
- Freezing bunch clock -- debugging
- How many Readout Supervisors?
- Jitter requirements for Readout Supervisor (TTCex)
- L0 rejects before reset to empty L0 derandomizer?
- L0 latency within RS