TFC Switch Specifications

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Abstract

In this paper we discuss we specify the functionality of the TFC switch.

Document Status Sheet

Table 1 Document Status Sheet

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1 Introduction

The LHCb Timing and Fast Control (TFC) system is described in [1]. The TFC switch is one of the components in the LHCb Timing and Fast Control (TFC) architecture (see Figure 1). It is needed in order to implement the partitioning concept in the LHCb DAQ and specifically in the TFC.

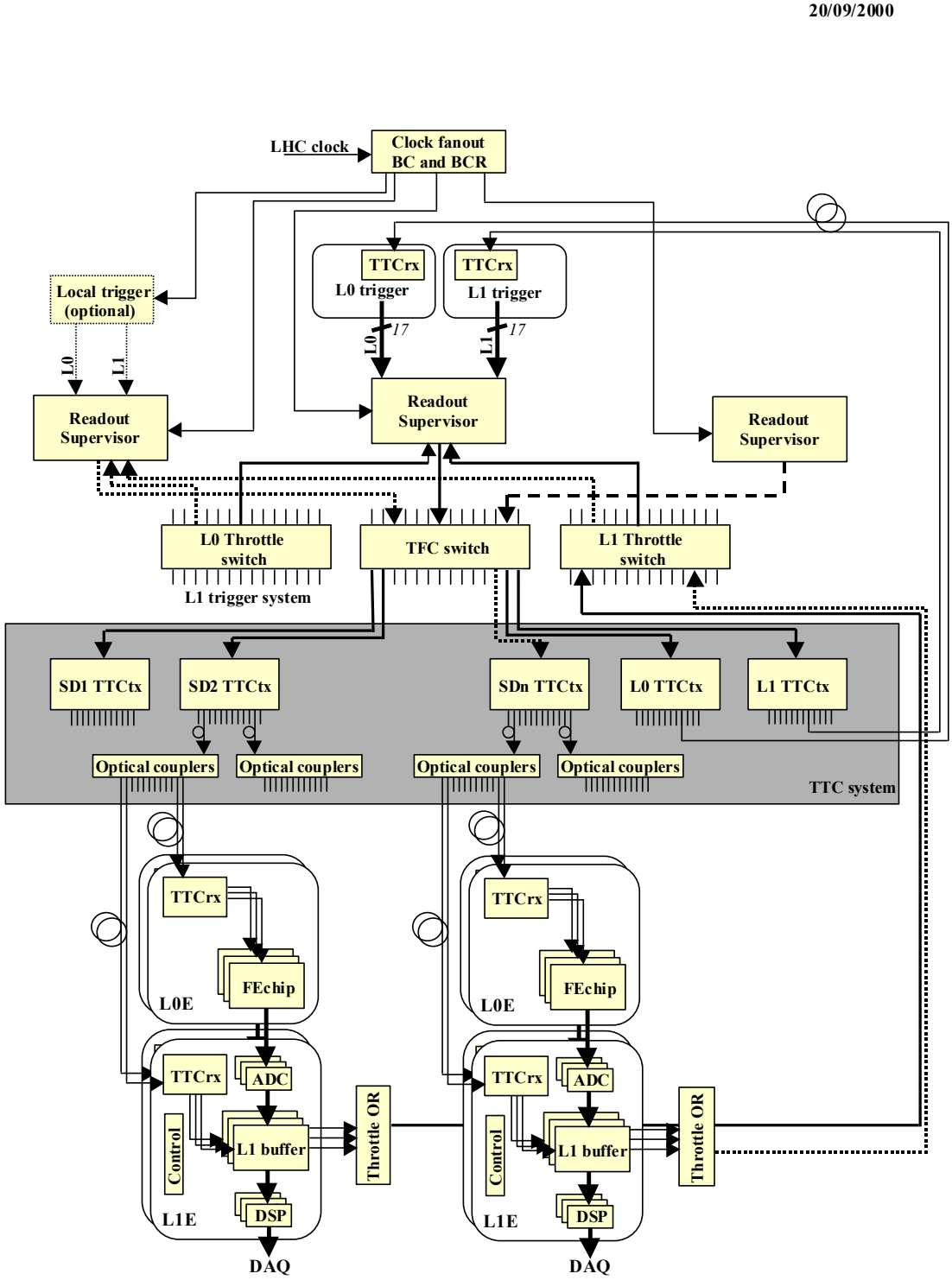

Figure 1 General Architecture of the LHCb TFC system

In Figure 2 the external interfaces of the TFC and the Throttle switches are shown

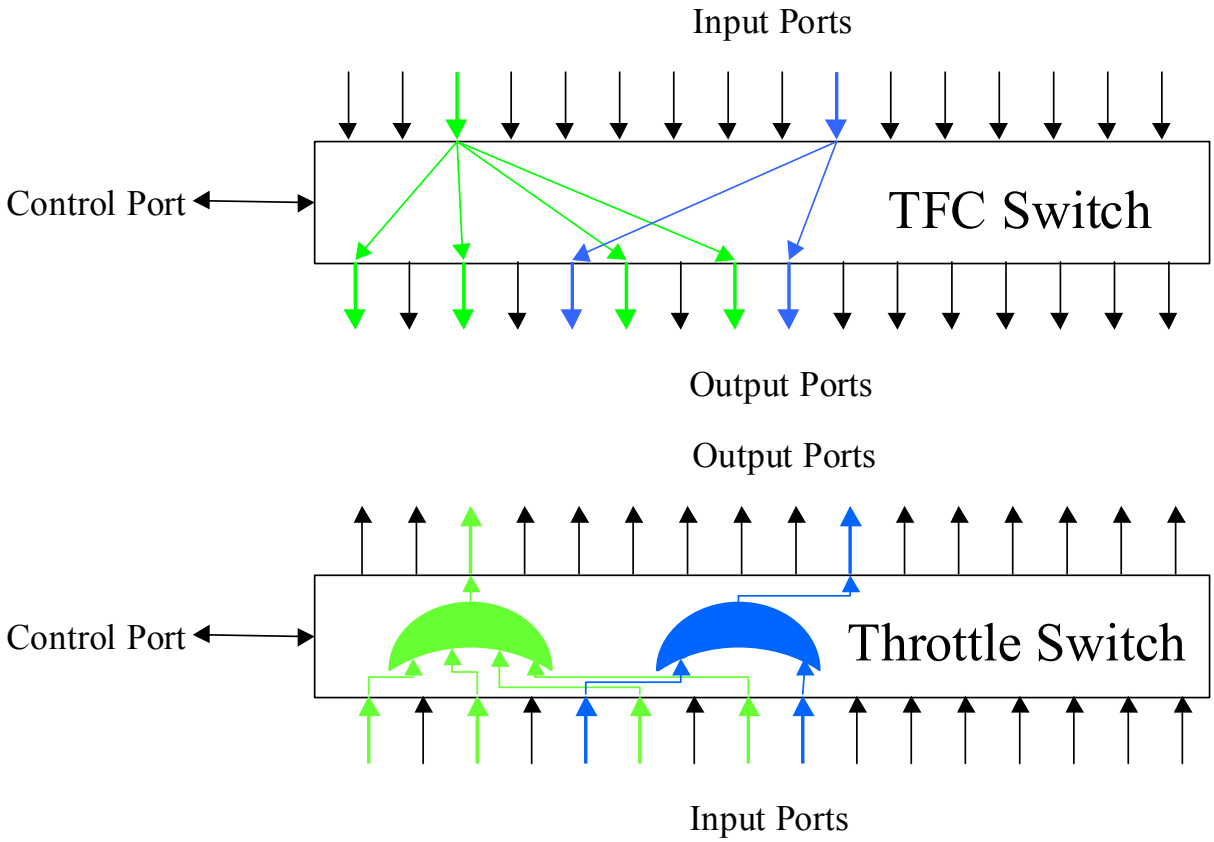

Figure 2 Schematic diagram of the external interfaces the TFC switch (upper diagram) and the Throttle switch (lower diagram) implement.

The TFC switch module should provide two types of interfaces to the external world

- A controls interface that allows to configure and monitor the module
- Input and output ports compatible with the RD12 TTC "standard" (see Ref. [2] for detailed information)

The Throttle switch module should implement the following two types of external interfaces

- A controls interface that allows to configure and monitor the module
- Throttle input and output ports. The characteristics of these will be defined soon.

2 Functional Specification

2.1 Introduction

The TFC Switch's function is to provide the connectivity between the sources of TFC signals, the Readout Supervisors (RS) and the TTC transmitters (TTCtx). This connectivity is not necessarily one-to-one, but rather one-to-many, i.e. the functionality needed is that of a Fan-out. It must be possible to select the connection remotely by software. No re-cabling should be needed to change the configuration. The TFC switch is not a switch in the network sense, but rather a programmable patch panel.
In addition a THROTTLE (Busy) signal has to be treated in the reverse direction, i.e. from the Front-End electronics or from the DAQ system to the RS, where the reverse association between inputs and outputs should be setup.
In the following we will call the path from the RS towards the TTCtx the **TFC Path** and the path of the throttle signals the **Throttle Path**.

2.2 Detailed Specifications

2.2.1 TFC Path

- The TFC switch will have 16 input and 16 output ports.
- The input ports should behave like the input port of the TTCtx and the output port like the output port of the RS, i.e. there should be no conversion electronics needed to introduce the TFC switch.
- The switch should be programmable through the control interface in such a way that any set of output ports can be associated to one input port. At any time the current configuration must be retrievable through the controls path.
- The setting-up of one path must not interfere with the operation of a path that is already set-up, i.e. if one set of output ports is being associated to an input port, no other already existing association must be disturbed in its operation.
- The phase difference between output ports of the same set should be less that 100 ps
- The additional jitter on the signal at the output should be less than 100 ps with respect to the input signals.
- The delay from input to output of the switch should be less than 10 ns.

In Table 2 The performance requirements on the TFC path are summarized.

Table 2 Summary of the performance specifications of the TFC Path of the switch

Item	**Specification**	**Comments**
Number of input ports	16	Or more
Number of output ports	16	Or more
Input/output port characteristics	Compatible with RD12 TTC	
Jitter introduced by switch	<100 ps	
Phase difference between output ports	<100 ps	
Delay from input to output	<10 ns	

At power up all ports (input and output) should be disabled and it should be possible to disable all or selected ports through the ECS port.

2.2.2 Throttle Path

The function of the throttle path is to allow components in the readout system (Front-End Electronics and DAQ) to throttle (inhibit) the issuing of positive trigger decision. These components will assert a throttle to prevent buffer

overflows in case the downstream data path is congested or blocked. The association of throttle inputs to throttle outputs is, under normal circumstances, identical to the association of TFC inputs to TFC outputs, i.e. if for example TFC input 1 is associated to outputs 1,3,6 and 16 then throttle inputs 1,3,6 and 16 must be associated to throttle output 1. There should however be functional independence between the throttle path and the TFC path, in that it should be possible to setup the throttle path independently from the TFC path.
Each throttle port will consist of two signals (Level-0 throttle and Level-1 throttle). The two throttle signals at the inputs must be ORed individually to form the appropriate throttle output signal. This means that the Level-0 throttle signal at the output must be the logical OR of the Level-0 throttle signals at the inputs and analogous for the Level-1 throttles. At any time the state of the throttle inputs and outputs must be readable via the controls interface.
Monitoring information is made available in the following way. At any transition of any port of a throttle signal, the state of all signals and the time of the transition are stored in a FIFO buffer. The ECS system will subsequently reconstruct the throttle history from the transitions in software.
The delay between the throttle inputs and throttle outputs should be less than 50 ns.
The implementation of the throttle ports is not yet decided. Potentially distances of up to ~70 m will have to be covered between the sources and the destinations of throttle signals. Possible technologies are either differential PECL or a very cheap optical link technology.

Table 3 Summary of the characteristics of the Throttle Path

Item	**Specification**	**Comments**
Number of input ports	16	Same number as TFC Path
Number of output ports	16	Same number as TFC Path
Input/output port characteristics	????	PECL, Optical?
Logical Operation	Output is Logical OR of inputs	L0/L1 separately
Monitoring		
Resolution	100 ns	
History	>32000 samples (FIFO)	Store transitions with time-stamp
Time-Stamp	>32 bits	Preferably 64 bits
Delay from input to output	<50 ns	

At power up all ports (input and output) should be disabled and it should be possible to disable all or selected ports through the ECS port.

2.2.3 Controls Path

The function of the controls path is to allow configuring and monitoring the TFC Switch. It should be implemented using the standard LHCb controls interface (TBS). Any function of the TFC Switch should be accessible through the controls interface. There should be no switches or other mechanical items on the board. The throttle history FIFO should be accessible at any time through the ECS interface, provided it is not empty.

2.2.4 Mechanical Implementation

The switches (TFC, L0 and L1 throttles) should be implemented in a modular fashion. Either as three piggy-back boards on a common mother board, or as three different modules (potentially rack-mounted).

2.3 Throttle OR module

The function of the Throttle OR module is to perform the logical OR of a number of inputs (e.g. 16) to one output. The inputs that participate in the ORing should be selectable via the ECS interface. The characteristics and specification of the Throttle OR are the same as for the Throttle switch (Throttle Path of the TFC switch), with the exception that there is only one output instead of 16. Power-up state and configurability are identical to the Throttle switch.

3 Glossary of Terms

FEE	Front-End Electronics, denoting a summary term for both the Level-0 electronics and the Level-1 electronics
Level-0 Electronics	It holds all the necessary components for processing and buffering the detector data for the latency of the Level-0 trigger. It also contains a de-randomising buffer to cope with the random arrival of Level-0 triggers and all electronics necessary for the transfer the data to the Level-1 electronics..
Level-1 Electronics	Off Detector Electronics. It hold the buffers for the data to bridge the latency of the Level-1 trigger and processing elements to perform Zero-Suppression.
TFC	Timing and Fast Control system of LHCb. It uses the TTC system but has a wider scope.
TTC	Trigger Timing and Control system developed in the framework of the RD-12 collaboration
TTCrx	TTC Receiver. A chip that receives the information from the TTCtx and recovers a synchronous clock and the Level-0 decisions. It also makes the contents of the Channel B broadcasts available.
TTCtx	TTC Transmitter. Unit to transmit the encoded TTC information through the optical distribution network

4 References

[1] Timing and Fast Control, LHCb Technical Note, LHCb DAQ 2001-016 (unpublished).

[2] RD-12 Documentation on WWW (http://www.cern.ch/TTC/intro.html) and references therein