Use of Network Processors in DAQ Systems

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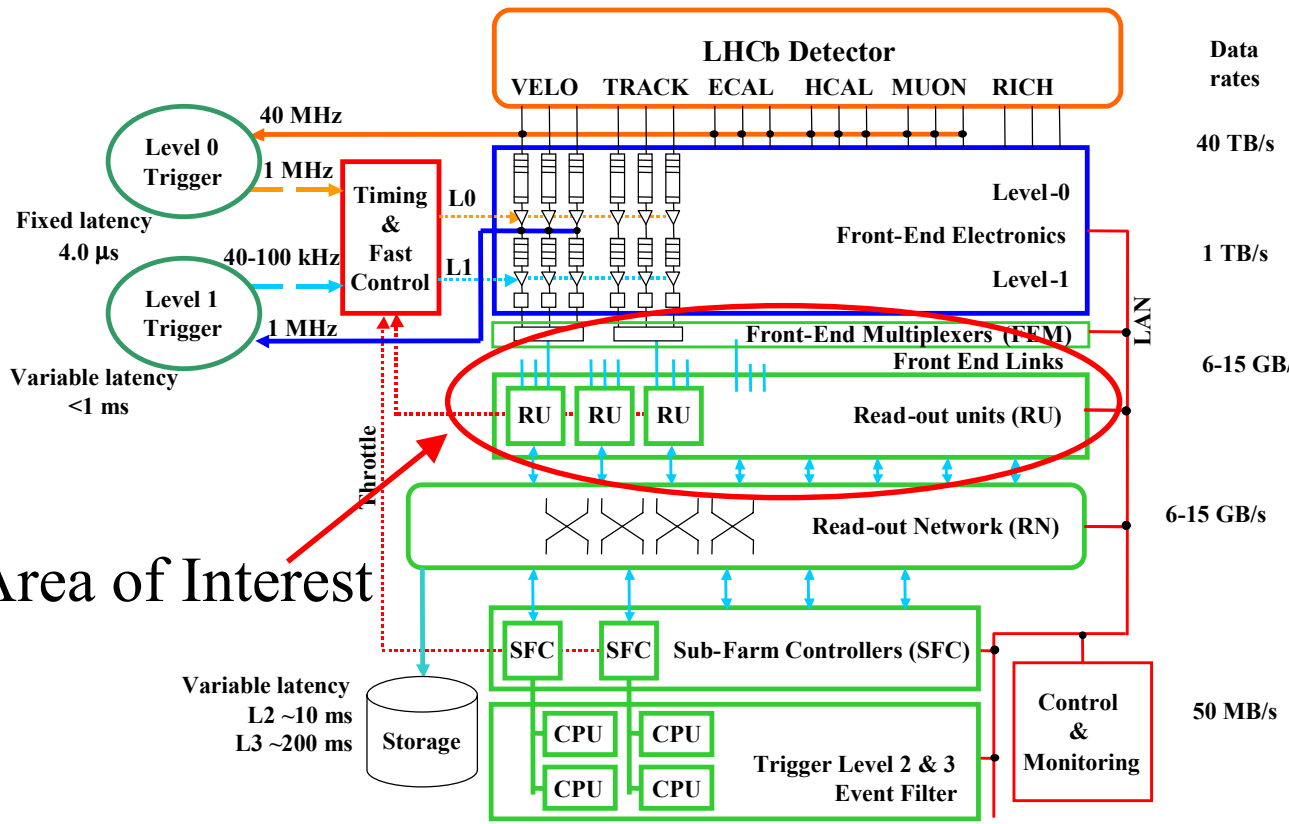
Outline

- Introduction
- What are Network Processors
- Application to Data Multiplexing/Merging
- Performance
- Conclusion

Introduction

LHCb DAQ Architecture



Data-Flow Requirements:

- L1-Rate: 40-100 kHz
- Event Size: ~150 kB
- Data Rate: 6-15 GB/s

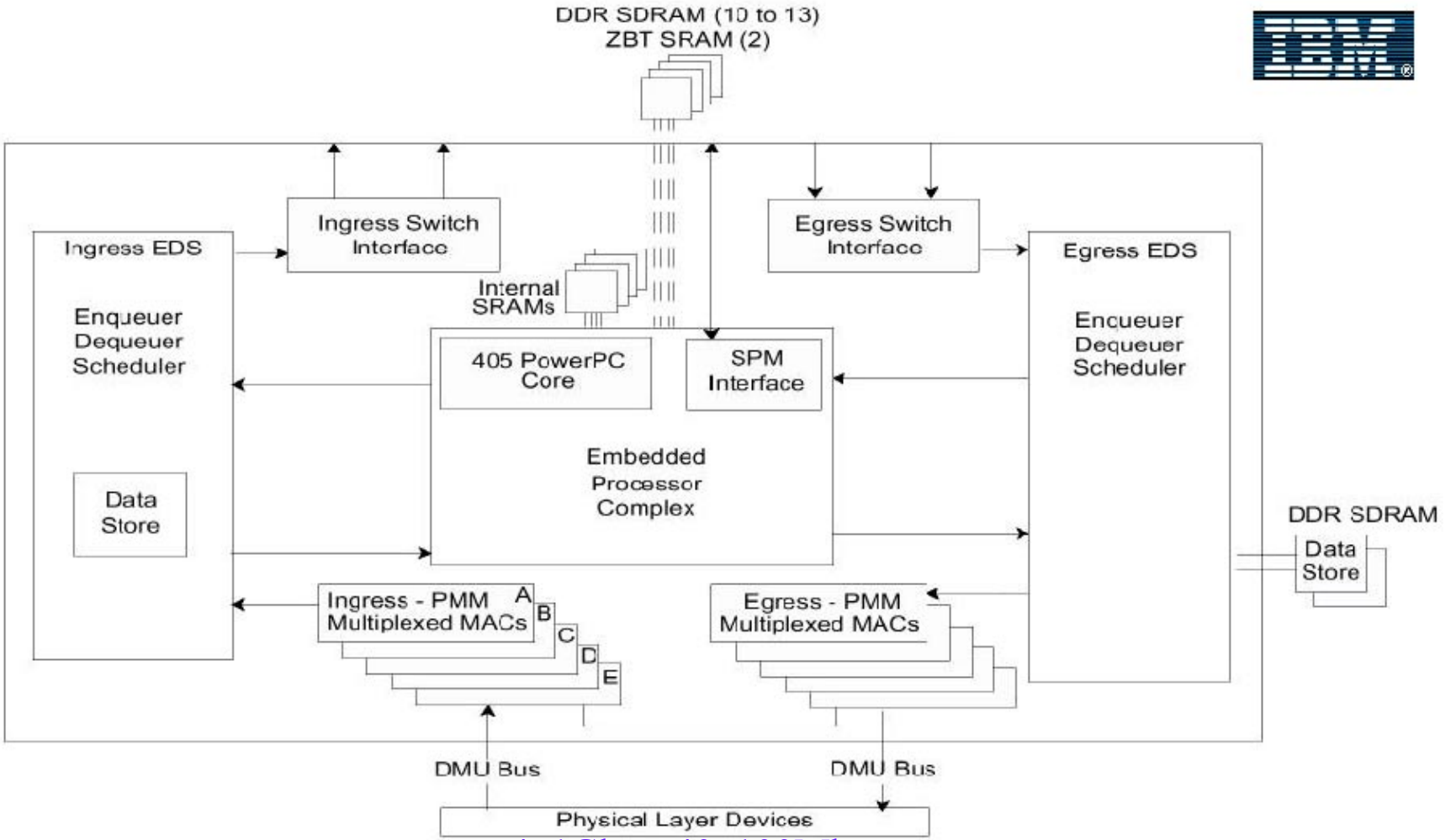
Multiplexing factors
In FEM/RU: ~4-16:1

Introduction to Network Processors

- Network Processors are a new technology gaining very much in momentum in the switch industry. All major chip manufacturers are working on them (IBM, Intel, Siemens, …)
- Target market are switch manufacturers using them as input stage of high-speed switches.
- Consisting of a set of RISC core processors (usually multithreaded in hardware) with specialized co-processors for functions like tree-lookup or checksum calculations, all on one chip
- RISC processors are specialized at frame manipulations

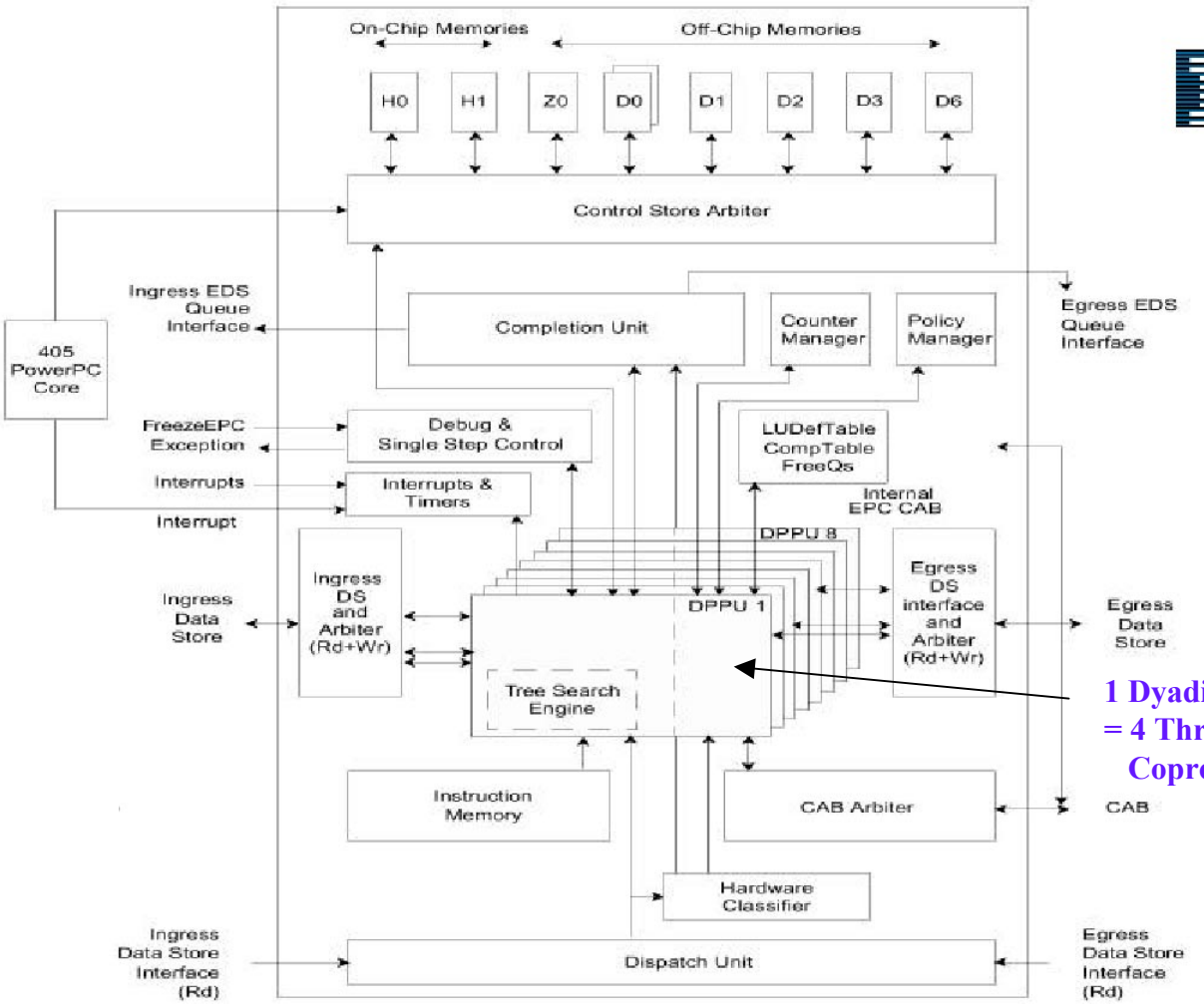
- We somehow abuse them for doing event-building (assembly of several data frames to one bigger one) in networked DAQ systems
- We focus for the time being on the IBM NP4GS3(B) Network Processor

General Architecture



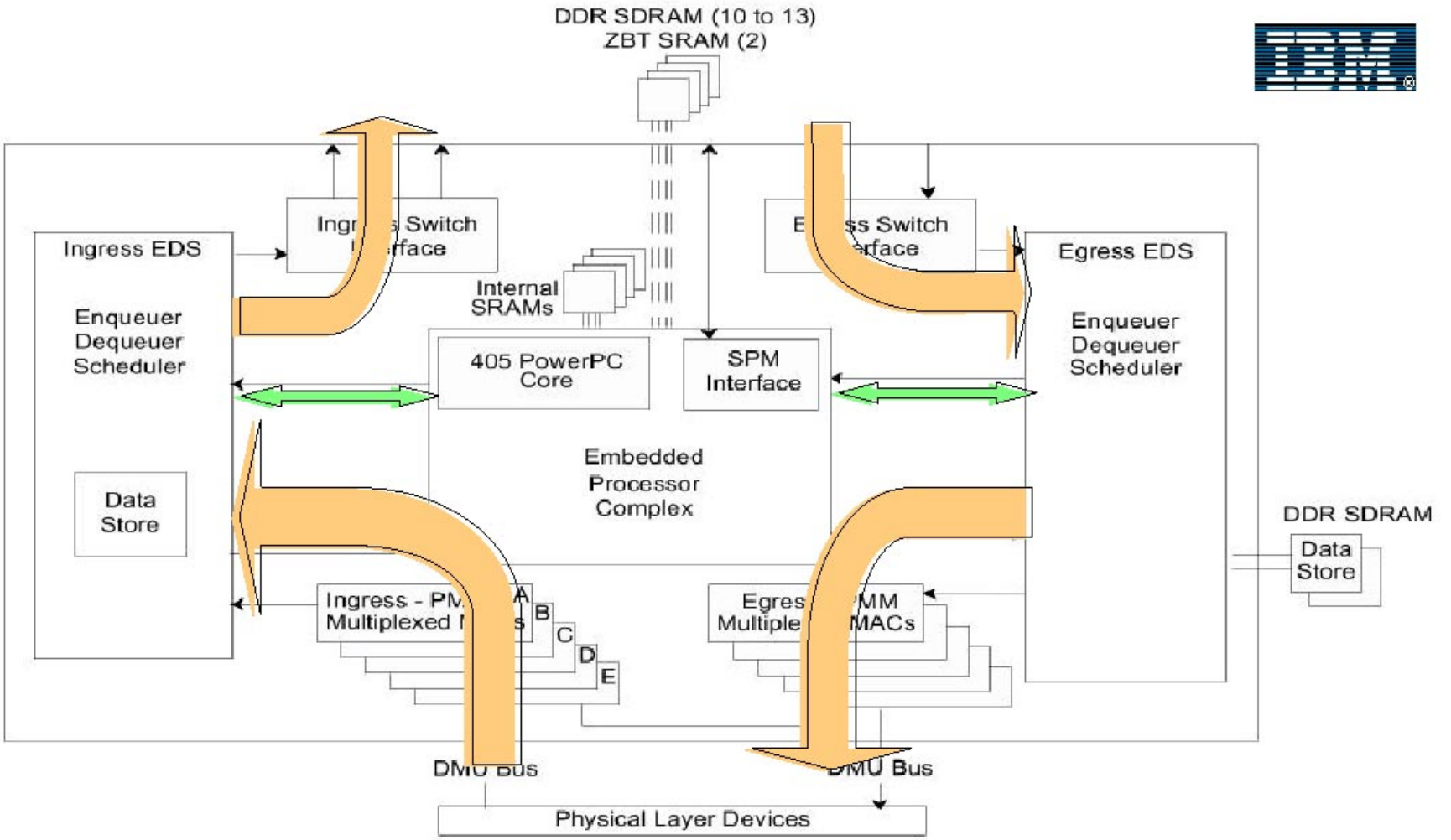
4x1Gb or 40x100Mb

Embedded Processor Complex



1 Dyadic Protocol Processor Unit = 4 Threads sharing one set of Coprocessors

Data Flow

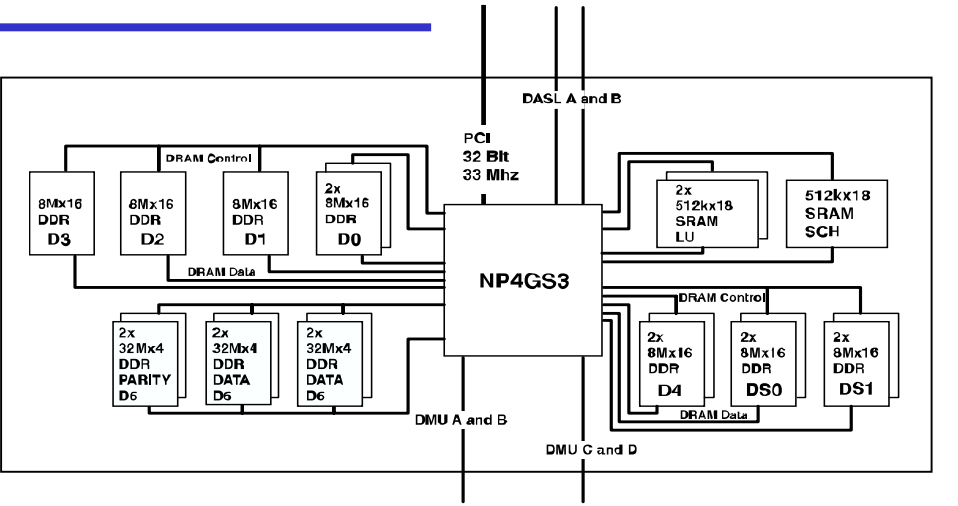

DDR SDRAM (10 to 13)
ZBT SRAM (2)
Ingress EDS
Enqueuer
Dequeuer
Scheduler
Data
Store
Internal
SRAMs
405 PowerPC
Core
SPM
Interface
Embedded
Processor
Complex
Egress EDS
Enqueuer
Dequeuer
Scheduler
DDR SDRAM
Data
Store
A
B
C
D
E
DMU Bus
DMU Bus
Physical Layer Devices

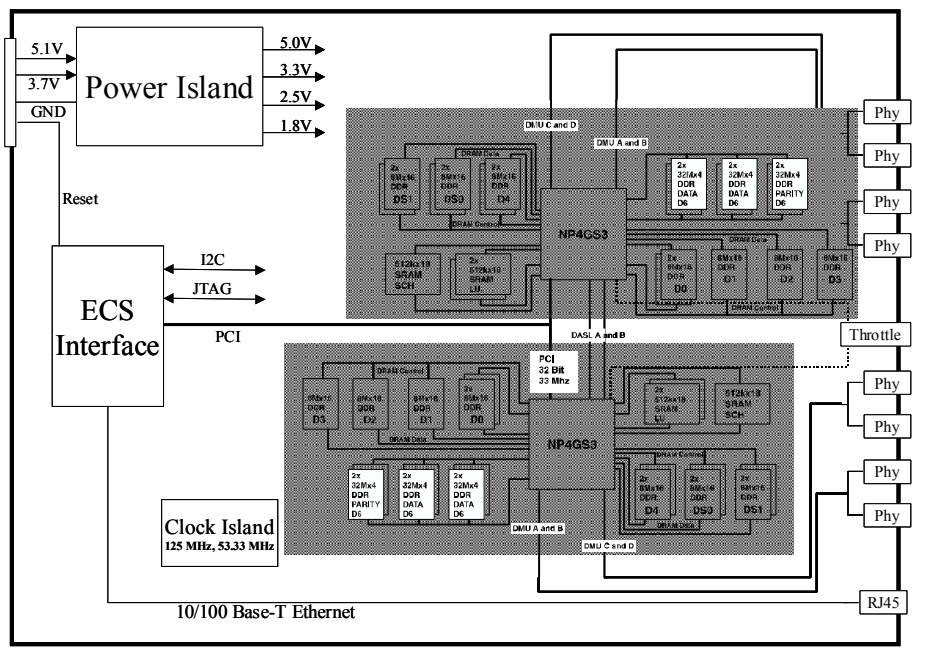
Development Environment and Experience

- There is a very elaborate development environment available, consisting of
  - Assembler
  - Simulator/Debugger
  - Profiler for performance studies
  - Reference hardware kit (equivalent in functionality to what we want to have on a board)
- Our experience is very positive
  - Without the simulator it is impossible to develop and test code (specially if there are problems with synchronization)
  - The performance measurements need to be confirmed with real hardware
  - There are still a few undesired features that will hopefully be ironed out eventually.

Board-Level Integration

- Only first ideas yet
  - Mezzanine Card with all the infrastructure of the NP (memories, etc…)
  - Carrier Board with all the infrastructure (Power, Clock) and the link to the controls system
  - Feasibility studies under way





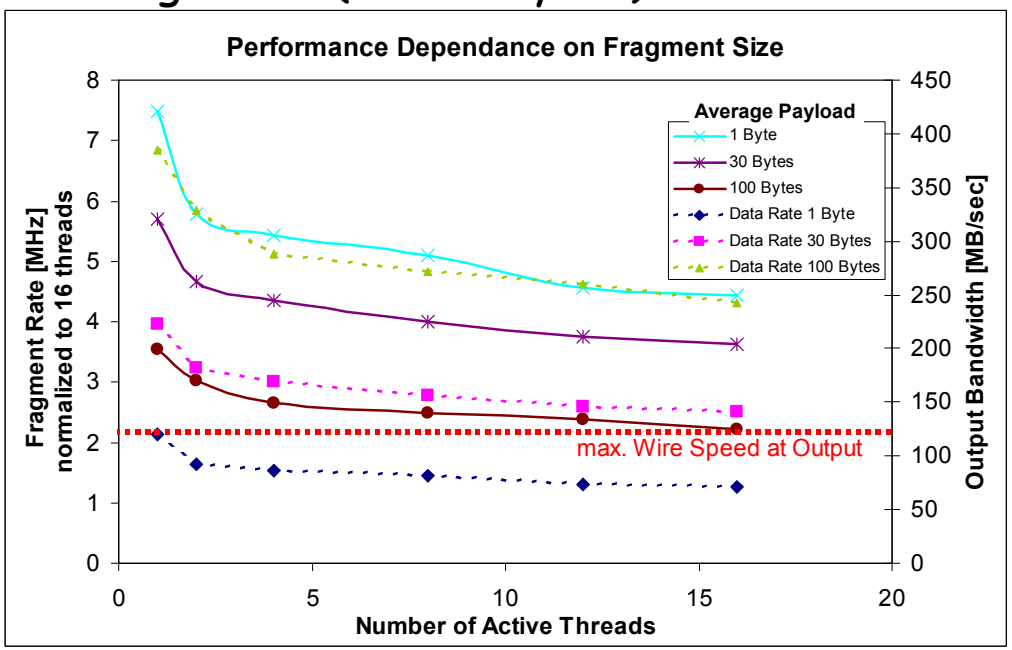
Possible Applications in LHCb

- The module envisaged is very generic. It could be used for
  - Front-End Multiplexing/Readout Unit
  - Building block for the readout network (8-port switch)
  - Final event-building element downstream of the readout network as a replacement of "smart NICs"
- Uniform Hardware. The software loaded determines the functionality

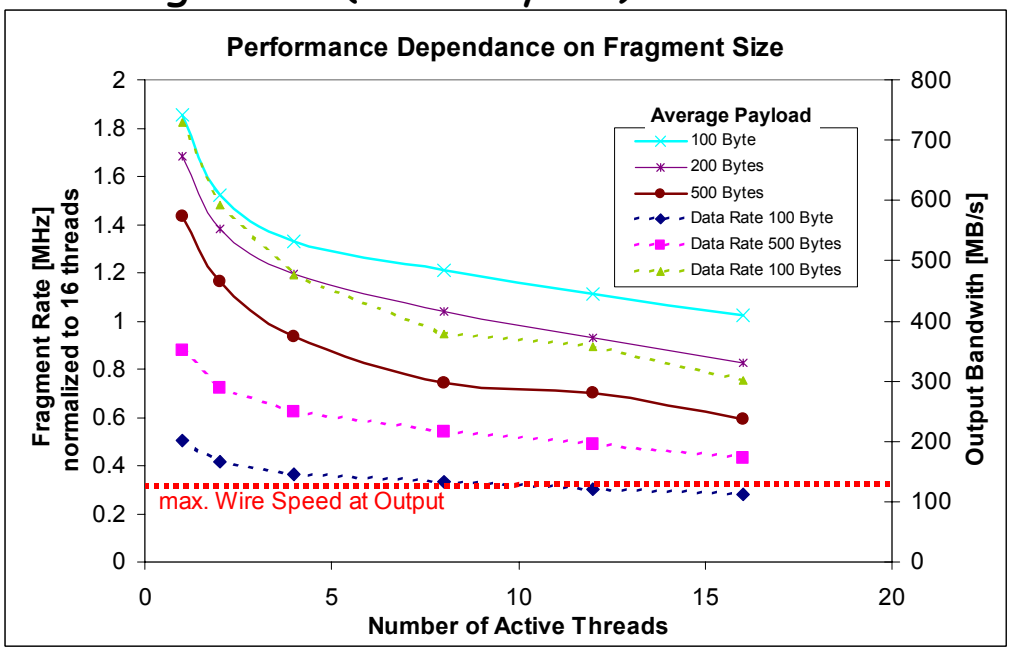
Performance for 4:1 Event-Building

Two versions of the code written, debugged and simulated (cycle precise) taking into account contentions for shared resources

Optimized for very small incoming fragments (30-60 Bytes)



Optimized for larger incoming fragments (~500 Bytes)



→For all practical purposes we achieve wire-speed event-building performance

Conclusion

- Network Processors are a promising technology to be applied to network-based DAQ systems
- We have outlined a generic module that could serve all functions throughout the LHCb DAQ System
- A very elaborate development environment is available
- The performance achieved with the first version of the code is shown by simulation to be largely sufficient for LHCb and we achieve wire-speed performance for all practical purposes

Profiler Information